TLCU-1
Traffic Management
Local Control Unit

User Manual

LOW POWER MODEMS LIMITED DISTANCE MODEMS LIGHT OUT DETECTORS
LOCAL CONTROL UNITS LOAD SWITCHES CUSTOM ENGINEERING

MICRO-AIDE

USER MANUAL

TLCU-1
LOCAL CONTROL UNIT

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CHAPTER 1

DESCRIPTION

Introduction

The TLCU-1 Traffic Management Local Control Unit (hereinafter referred to as the LCU) is a Z80 microprocessor-based, STD Bus computer product designed to provide distributed control functions as part of an advanced traffic management system.

The LCU was designed at the specific request of the Texas Department of Transportation (TxDOT). **It is important to note that the LCU as manufactured and delivered by MICRO-AIDE is a hardware-only product**. The LCU is fully compliant with all hardware-related specifications and requirements currently defined by TxDOT. Accordingly, MICRO-AIDE is not responsible for any of the application and/or test firmware that may be installed by the user into the LCU.

General Description

The LCU is housed in a rigid, industrial grade chassis fabricated from aluminum. It is rated for operation over a temperature range extending from -34ºC to 74ºC (-29ºF to 165ºF).

Note To insure operation over the broadest possible temperature range, CMOS series 74HCTxx, 74ACTxx and/or other CMOS components have been substituted for 74LSxx and other TTL components throughout the design of the LCU.

Front Panel

The LCU's front panel is hinged to allow for 180º of rotation. Several switches, indicators and connectors are mounted on the front panel. A DB-25 connector labeled "Communications Port" can be used to provide serial data communications through an external modem. A second DB-25 connector labeled "Diagnostic Port" can be connected to any Data Terminal Device (e.g., PC or printer) for system verification purposes.

Four AMP 206438-1 connectors allow interconnection to the LCU's 119 signal inputs and 72 signal outputs. All signal inputs and outputs are optically isolated from other electronic circuitry, power sources, ground and chassis metal work. The signal inputs and outputs can be used to monitor various roadway sensors and switches, as well as to control message signs and cameras.

An AMP 206705-1, nine-pin connector labeled "Power" is used to connect to a 120Vac/60Hz power source. The power switch can be used to turn power on and off. Three Light Emitting Diodes (LEDs) are used to indicate the status of the LCU's 5, 12 and -12Vdc internal power. A

fourth LED labeled "On Line Status" is used to indicate that signal outputs are active. The "On Line Enable" switch provides direct control of the signal outputs.

A 16-position push wheel switch labeled "Channel Address" allows the user to assign a distinct Unit ID to any individual LCU. The "Reset" switch can be used to restart execution of the internally stored firmware.

Rear Panel

The rear panel of the LCU includes a simplex 120 Vac outlet. The outlet is fused, but not switched. It can be used to provide power to an external device (e.g., MICRO-AIDE Limited Distance Modem).

Printed Circuit Boards

The LCU is equipped with 11 plug-in printed circuit boards (PCBs). The 11 PCBs are listed in the following table. Each PCB is briefly described in the sections that follow the table.

PCB Card Slot	Qty.	Part Number	Name
1 or 2 (recommended)	1	80-0026	CPU
2 or 3 (recommended)	1	80-0042	Watchdog Timer
4-8	5	80-0023	Opto-Input (24 inputs per PCB)
9-11	3	80-0030	Opto-Output (24 outputs per PCB)
13	1	80-0041	Power Supply

Table 1 - Printed Circuit Boards

Tip MICRO-AIDE recommends that the CPU PCB be inserted into card slot 2. The CPU's flat-wire cables clear the front panel with greater clearance if it is installed into slot 2.

CPU

The 80-0026 CPU provides a complete Z80-based microcomputer on a single STD Bus card. It meets all STD Bus requirements and fully supports all Z80 and 8080 instructions. It includes an on-board UART for control of both RS-232 serial ports, four independent timer/counters and a parallel I/O port. I/O addresses of the peripheral controllers are mapped by a small PROM device. The latter can be modified by the user to suit specific requirements. Four 28-pin sockets are designed to accept RAM, EPROM and EEPROM devices of ranging from 2 KB to 32 KB.

Watchdog Timer

The 80-0042 Watchdog Timer provides a complete event monitoring system. It is STD Bus compliant. The control signals, address bus and data bus are fully buffered to insure improved performance of the STD Bus.

Opto-Input

The 80-0023 Opto-Input includes 24 optically isolated inputs. The state of each input can be read by the CPU in three groups of eight. Each input is protected against excessive current and voltage. A 4N33 opto-isolator device is used to provide electrical isolation from internal and external power and ground sources.

Opto-Output

The 80-0030 Opto-Output allows the CPU to control the state of each output. The 24 optically isolated outputs can be controlled individually. They are accessed in three groups of eight. The flow of output current is further controlled by the state of a single relay whose contacts are common to all 24 outputs.

Power Supply

The 80-0041 Power Supply utilizes series-pass regulation in its design. This eliminates noise generally associated with switching power supplies. It can provide 5, 12 and -12 Vdc at 3, .5 and .5 A of current, respectively. Each output is protected against overload conditions.

The next chapter provides a detailed theory of operation and list of design specifications for each of the LCU PCBs.

About This Manual

The content of this manual is limited to a description of the LCU hardware. MICRO-AIDE has never designed and is therefore not responsible for any application firmware executed by the LCU. Furthermore, MICRO-AIDE does not ship its LCU with pre-installed firmware. Specifically, the contents of the EPROM and EEPROMs installed in the CPU PCB are blank. MICRO-AIDE tests its LCU with TxDOT provided diagnostic firmware and warrants that it will perform in accordance with all hardware specifications and requirements as stated herein.

Assistance with LCU hardware-related issues should be directed to MICRO-AIDE. Additional copies of this manual are available upon request.

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Note The MICRO-AIDE Material Return and Limited Warranty policies can be found on the inside back cover of this manual.

Change Notices

This manual has been written to include several Change Notices that had been included as addenda inserts within previous manuals. Specifically, the following Change Notices have been included.

• Change Notice dated February 10, 1999, referring to general changes made to the design of the LCU.

• Change Notice dated July 1, 2001, referring to how the CPU Reset signal is now synchronized to the CPU 12.288 MHz clock.

• Change Notice dated July 1, 2001, referring to the design and use of the 85-0086 Switch Interface Circuit.

User Notes

CHAPTER 2

THEORY OF OPERATION

Introduction

The LCU is comprised of several STD Bus compliant PCBs. The design of each PCB is described in this chapter. The theory of operation is also described. Wherever possible, diagrams and design specifications are included.

PCB Descriptions

80-0026 CPU Rev E

Features

The 80-0026 CPU provides a complete Z80-based microcomputer on a single circuit board. It meets all STD Bus requirements and fully supports all Z80 and 8080 instructions. The board includes the following important components:

- CMOS Z80B CPU
- CMOS Z80B CTC Timer
- CMOS Z80B SIO serial controller, accommodating two fully implemented RS-232C serial ports with EIA drivers and receivers
- Four 28-pin sockets with jumpers for use with 2K to 32K JEDEC compatible RAM, EPROM and EEPROM devices

The components described above and all other supporting components operate with no wait states and an oscillator frequency of 12.288MHz. The CPU fully supports DMA transfers to and from on-board memory. A special control register is used for software control of external I/O and memory. A Boot Prom Enable/Bank Enable control signal provides for bank switching of off-board memory. A functional block diagram of the CPU PCB is included in Figure 1 on page 6.

Four standard memory configurations are selected via two jumpers (S1-S2). They control the memory mapping PROM. The latter may be modified by the user for special applications. The I/O mapping of the Z80 CTC timer, Z80 SIO, and port C (parallel port) are also under PROM control allowing them to be mapped anywhere in the Z80 I/O address space.

Note The 80-0026 CPU is designed for considerable flexibility. It can be configured to support a broad range of STD Bus applications. However, this manual refers to revision E of the 80-0026 CPU PCB as it is used in the LCU. Revision E includes a change to synchronize the reset signal with the CPU clock. The CPU clock was changed to 6.144MHz.

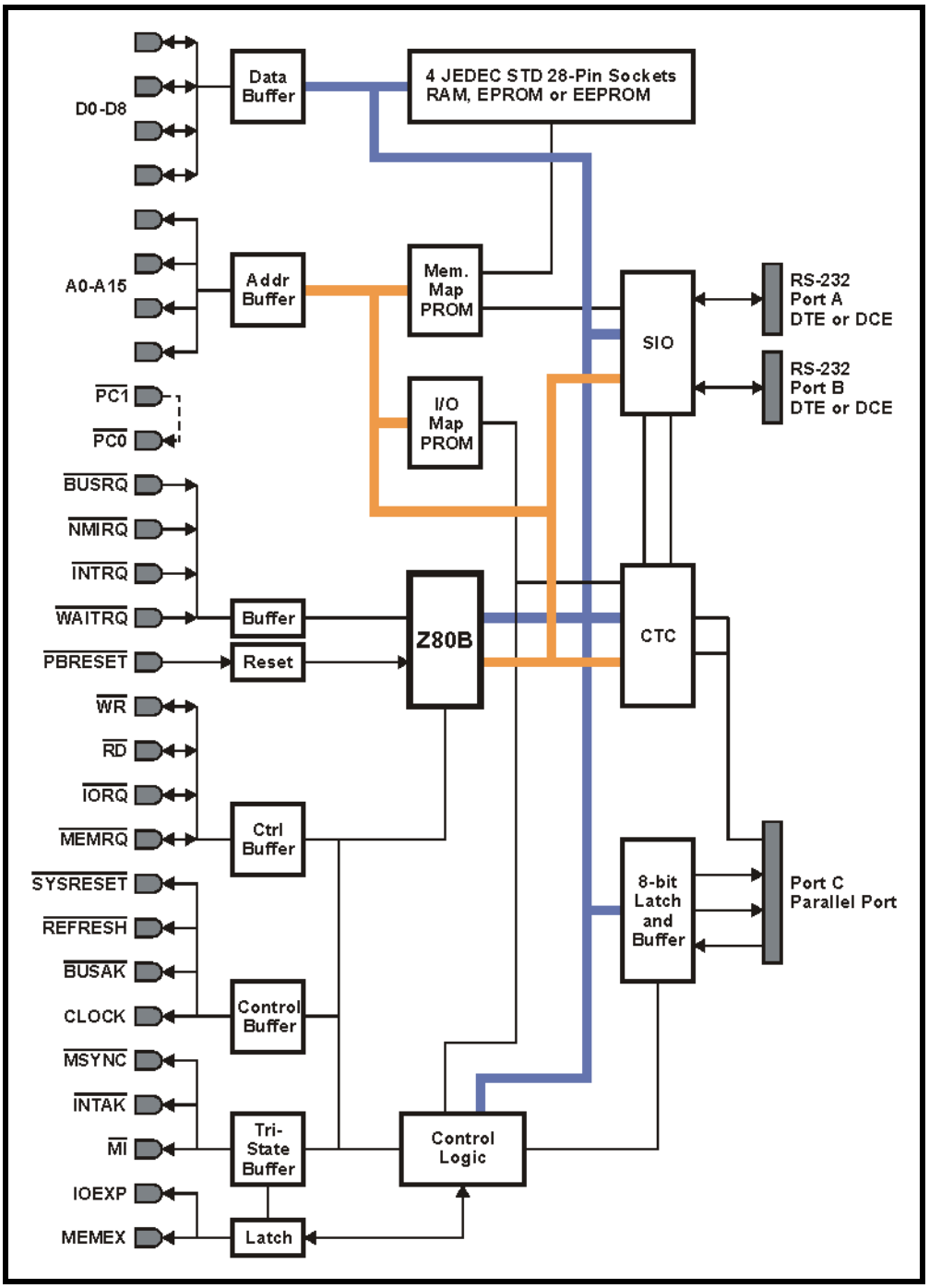


Figure 1 - Functional Diagram of 80-0026 CPU

Factory Configuration

The memory mapping PROM is factory programmed to decode four consecutive blocks of memory. Each memory block is sized as 8K by 8-bits. A 28-pin DIP socket is provided for each memory block. The first socket is jumpered for a 27C64 CMOS EPROM occupying address locations 0000H through 1FFFH. Address locations 2000H through 3FFFH are reserved for

the second socket. It is jumpered for an 8K by 8 static CMOS RAM. The third socket is assigned to address locations 4000H through 5FFFH. It can accommodate a low power 28C64 EEPROM. The last socket occupies address locations 6000H through 7FFFH. It can accommodate a second low power 28C64 EEPROM. Figure 2 depicts the 80-0026 CPU in the exact configuration required by the LCU. Specifically, the complement of memory devices (i.e., RAM, EPROM and EEPROM) and jumper settings reflects the LCU application.

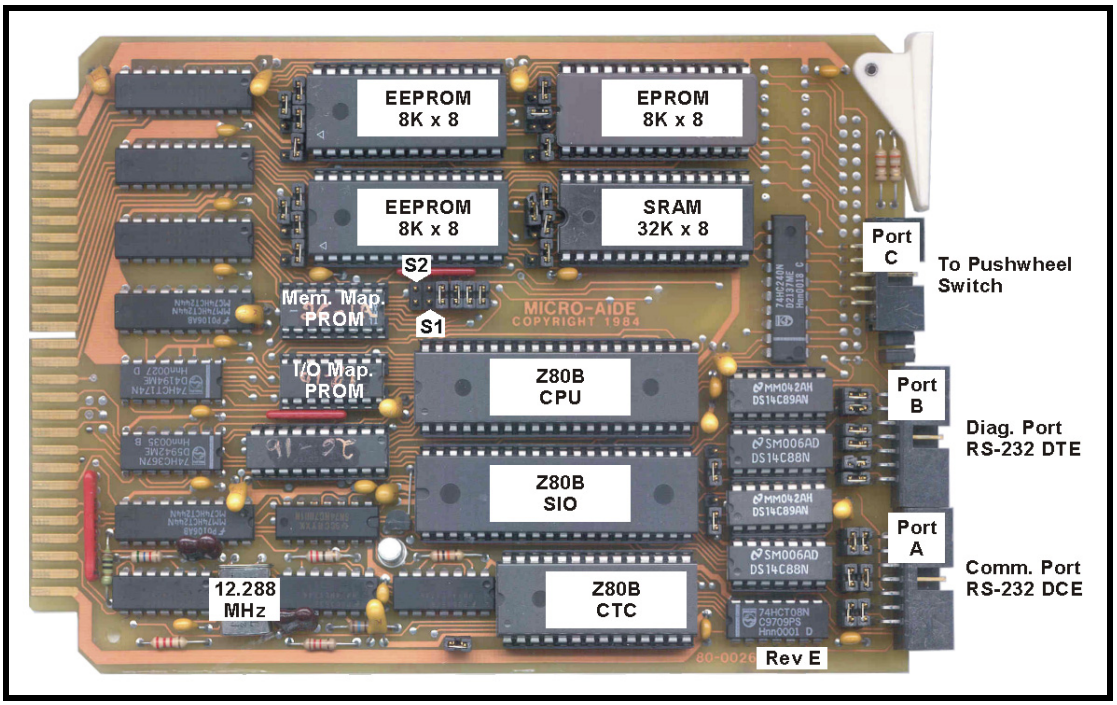


Figure 2 - 80-0026 CPU

Note Because of availability, a 32KB RAM is used in the RAM socket. The upper 24KB are ignored.

Table 2 describes how the I/O address space is decoded by the I/O mapping PROM.

I/O Address	Function
78H	SIO channel A data
79H	SIO channel A command
7AH	SIO channel B data
7BH	SIO channel B command
7CH	CTC timer channel 0
7DH	CTC timer channel 1
7EH	CTC timer channel 2
7FH	CTC timer channel 3
FEH	Port C (parallel I/O port)
FFH	reserved for MEMEX/IOEXP control

Table 2 - I/O Mapping PROM

The lower four bits of the CPU board's port C are terminated in a 10-pin header connector. The bits are used to read the binary coded value of the push wheel switch located at the front panel of the LCU. The signals identified as I0, I1, I2 and I3 in the 10-pin header connector are connected to the binary 1, 2, 4 and 8 outputs of the push wheel switch, respectively.

The state of the Online Enable switch is also read via port C as I4.

Operating Instructions

This section briefly describes the operating instructions of the 80-0026 CPU. Baud rates, I/O assignments and installation of EPROMs and RAMs are included. General operating characteristics are also described.

Z80B CPU

The 80-0026 CPU utilizes the Z80B microprocessor. Accordingly, it supports all of the standard operating instructions and timing characteristics of the device. It is clocked at 6.144MHz. Refer to Zilog's Z80B documentation for additional information.

Z80B CTC

The 80-0026 CPU utilizes the counter/timer C0 and C1 for generating Baud rates used by serial ports A and B, respectively. The C2 and C3 counter/timers remain available for software timing, external counting and interrupt functions. In its standard configuration the CTC is located at I/O addresses 7CH through 7FH. However, it can be relocated to any four consecutive I/O addresses by changing the I/O mapping PROM.

Only two of the four CTC counter/timers are used by the LCU version of the CPU card. They are used as follows:

• Timer 0: Generates the Baud rate for port A. It is pin 7 of the Z80B CTC.

• Timer 1: Generates the Baud rate for port B. It is pin 8 of the Z80B CTC.

Timer Setup: To set up the timer interrupts, an interrupt map with a starting address divisible by eight is used. Each timer requires two bytes of branching address. Eight bytes total are required by the four timers. The interrupt map cannot straddle a memory page boundary. The interrupt mode of the Z80B uses only the high order byte of the interrupt map. The low order byte of the address is programmed into the CTC. During an interrupt, the CPU fetches the high and low order bytes and uses them to index into the interrupt map to obtain the starting address of the interrupt servicing routine.

Baud Rates: The CTC may be programmed to generate various Baud rates by writing two bytes of data into the corresponding CTC registers. Table 3 on page 9 lists the correspondence between register values and Baud rates.

Baud Rate	Byte 1	Byte 2
110	05H	D5H
300	05H	4EH
1200	45H	9CH
2400	45H	4EH
4800	45H	27H
9600	45H	14H
19,200	45H	0AH

Table 3 - Baud Rate Settings

I/O Addresses: The standard I/O address assignments for the CTC are listed in Table 4.

I/O Address	Function
7CH	CTC 0: Port A Baud rate
7DH	CTC 1: Port B Baud rate

Table 4 - CTC I/O Addresses

For more information, refer to the Zilog documentation provided for the Z80B CTC chip.

Z80B SIO

The 80-0026 CPU can accept either a Z80B SIO (synchronous/asynchronous serial I/O) chip or Z80B DART (dual asynchronous serial I/O) chip. A clock source strapping option is provided for each port. An internal clock provided by the CTC is used to clock the SIO chip in asynchronous operation. The LCU utilizes this mode of operation.

The signals used by serial ports A and B are connected to a pair of standard DB-25 connectors. EIA signal levels are used throughout both ports. A pair of jumper fields allow each port to be configured for either DCE or DTE operation.

The SIO is normally mapped at I/O addresses 78H through 7BH. However, it can be mapped to any four contiguous address locations by changing the I/O mapping PROM. The status of SIO can be monitored by accessing I/O registers. The SIO and CTC share similar interrupt handling routines. Within the interrupt handling routine the complete status of the SIO can be determined. This includes identification of the data source or destination.

The standard I/O address assignments for the SIO are listed in Table 5.

I/O Address	Function
78H	Port A data
79H	Port A command
7AH	Port B data
7BH	Port B command

Table 5 - DART/SIO Address Assignments

For more information, refer to the Zilog documentation provided for the Z80B SIO chip.

CTA and SIO Interrupt Priorities

The 80-0026 CPU is designed to fully support the STD Bus PC1 and PC2 features. The IE1 and IE0 signals of the CTC and SIO are daisy chained and interconnected as illustrated in Figure 3. The SIO is given priority over the CTC. Each PCB is given priority based upon its position in the card cage.

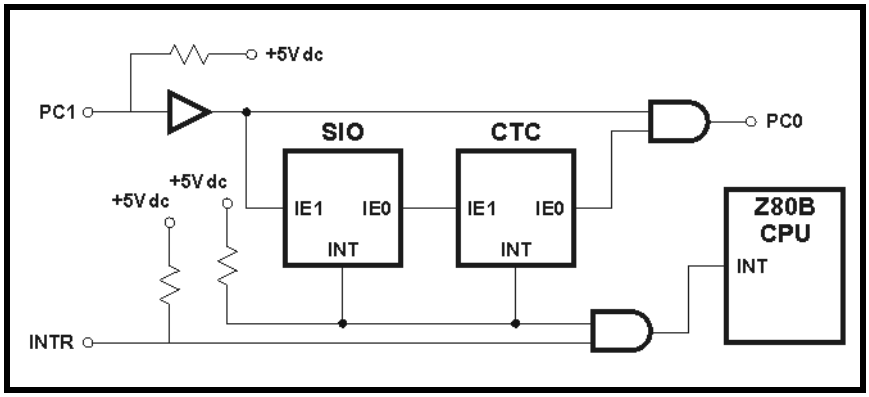


Figure 3 - CTC and SIO Interrupt Connections

Control Register

The 80-0026 CPU has a control register located at I/O address FFH. This register uses the lower three bits (i.e., D0, D1 and D2) for controlling the functions as described in Table 6.

Bit	Function	Description
D0	/MEMEX	Used for memory expansion beyond 64 KB. May be strapped to ground. Exp. memory is deselected with logic 1.
D1	/IOEXP	Used for I/O expansion. Normally low. May be strapped to ground.
D2	/BOOT ENABLE - /BANK LINE	Normally low. Memory mapping PROM may be programmed for bank selecting or as a boot enable.

Table 6 - Control Register Bits

Note At power-up or after a reset the I/O register will set all bits to a logic 0 state.

Port C (Parallel I/O Port)

The 80-0026 CPU provides a general purpose 8-bit I/O port which is located at I/O address FEH. Four of the eight input bits are brought out to a 10-pin header connector. A 10-conductor ribbon cable connects the port to the push wheel switch mounted on the LCU's front panel. It is also used to read the status of the Online Enbable switch.

Memory

The 80-0026 CPU includes four 28-pin sockets that can accept any combination of 2 KB, 4 KB, 8 KB, 16 KB or 32 KB RAMs, PROMs, EPROMs and EEPROMs that conform to the JEDEC pin out specifications. Refer to Figure 4 on page 11 for additional details.

Memory Map: The memory mapping PROM controls the memory address space. Two jumpers (S1 and S2) are used to select the memory configuration used by the mapping PROM. Jumper settings are depicted in Figure 2 on page 7. Table 7 lists the memory address space for the standard mapping PROM as used in the LCU version of the CPU card.

Address Input			Socket Position			
A7	A6	A5				
Bank Boot	S2 jumper	S1 jumper	0	1	2	3
0	On	On	2KB	2KB	2KB	2KB
0	On	Off	2KB	2KB	4KB	4KB
0	Off	On	4KB	4KB	4KB	4KB
0	Off	Off	8KB	8KB	8KB	8KB
1	On	On	not available	2KB	2KB	2KB
1	On	Off	not available	2KB	4KB	4KB
1	Off	On	not available	4KB	4KB	4KB
1	Off	Off	not available	8KB	8KB	8KB

Table 7 - Standard Memory Mapping PROM

Note Other memory mapping PROMs are available upon request.

DMA Transfer: When the processor receives an active BUSRQ signal it will assert the BUSAK signal after it completes the current machine cycle. A DMA device will have control of the STD Bus when the BUSAK signal is active. At the end of the DMA cycle the SMA will release the BUSRQ signal. Control of the STD Bus will return to the CPU.

RAM, EPROM and EEPROM Installation

The memory sockets of the 80-0026 CPU will accept 24- and 28-pin static RAM, EPROM and EEPROM devices that conform to the JEDEC pin out specifications. A 24-pin device can be installed in the socket as illustrated in Figure 4. Each socket has a jumper field that can be set to accommodate devices of various types and sizes.

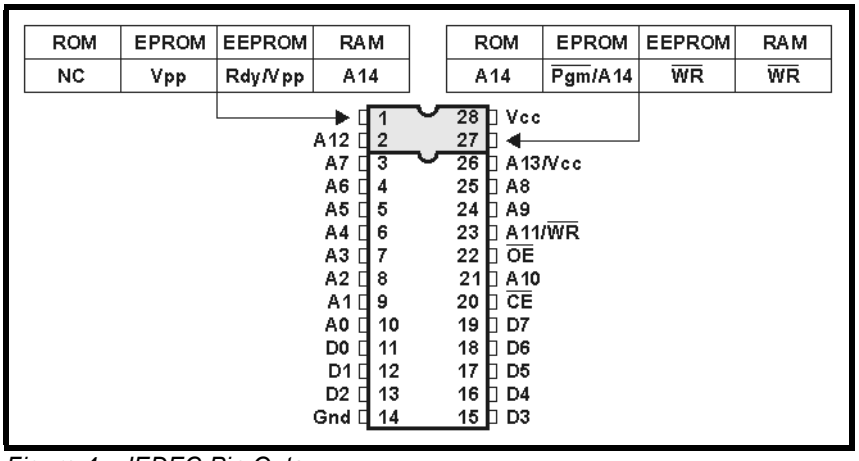


Figure 4 - JEDEC Pin Outs

80-0042 Watchdog Timer

Features

The 80-0042 Watchdog Timer can be used to perform a sanity check of the LCU. Additionally, it can be used to provide a remotely controlled system reset of the LCU. It is designed to be compliant with all STD Bus requirements. The various control signals, address and data busses are fully buffered to improve bus isolation. The card may be configured for operation in 8-bit I/O addressing mode, 16-bit I/O addressing mode or 16-bit memory addressing mode. Two jumper fields select the mode of operation. A fault condition can be reported to the CPU by means of a system reset or a non-maskable interrupt.

The Watchdog Timer includes a dual address space monitor. The address lines of the STD Bus are monitored to see if a specific illegal address has been issued. A second specific address is continuously monitored to provide a refresh signal to a time-out circuit. A third monitor looks for the presence of a break signal from the receive data of the CPU's port A (i.e., communications port). Two jumper fields control the interval of the address refresh and break signal duration.

Factory Configuration

Several jumpers and switches control the operation of the dual address space monitor. They are referred to as the illegal and refresh address monitors. Both are set for operation in 16-bit address mode. Jumper fields AX2 and AX4 control the mode of operation, respectively. Table 8 lists the default address settings.

Function	Address Bits																Hex Eq.
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
	Switch SW2								Switch SW1								
Illegal Address	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	8100H
	Switch SW4								Switch SW3								
Refresh Address	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8000H
Switch closed: 0 Switch open: 1																	

Table 8 - Address Space Monitor - Factory Settings

As indicated in Table 8 any access to address location 8100H will generate an immediate alarm condition. Conversely, address location 8000H must be accessed periodically and within a specified time interval to avoid a similar alarm condition. The refresh interval is set by jumper field AX5. Its factory setting is 1.0 seconds.

The receive data from port A is monitored for a break signal. The duration of the break signal is set by jumper field AX7. Its factory setting is .5 seconds. Port A of the 80-0026 CPU can be set to operate as a DTE or DCE port. DCE is the factory default setting. Accordingly, jumper AX6 on the Watchdog Timer is set to monitor a DCE configured port.

The type of alarm condition generated by the dual address and break signal monitors is set by jumper AX1. It can be set for either NMI (non-maskable interrupt) or system reset operation. System reset is the factory default setting.

Figure 5 depicts the various factory default jumper and switch settings of the Watchdog Timer.

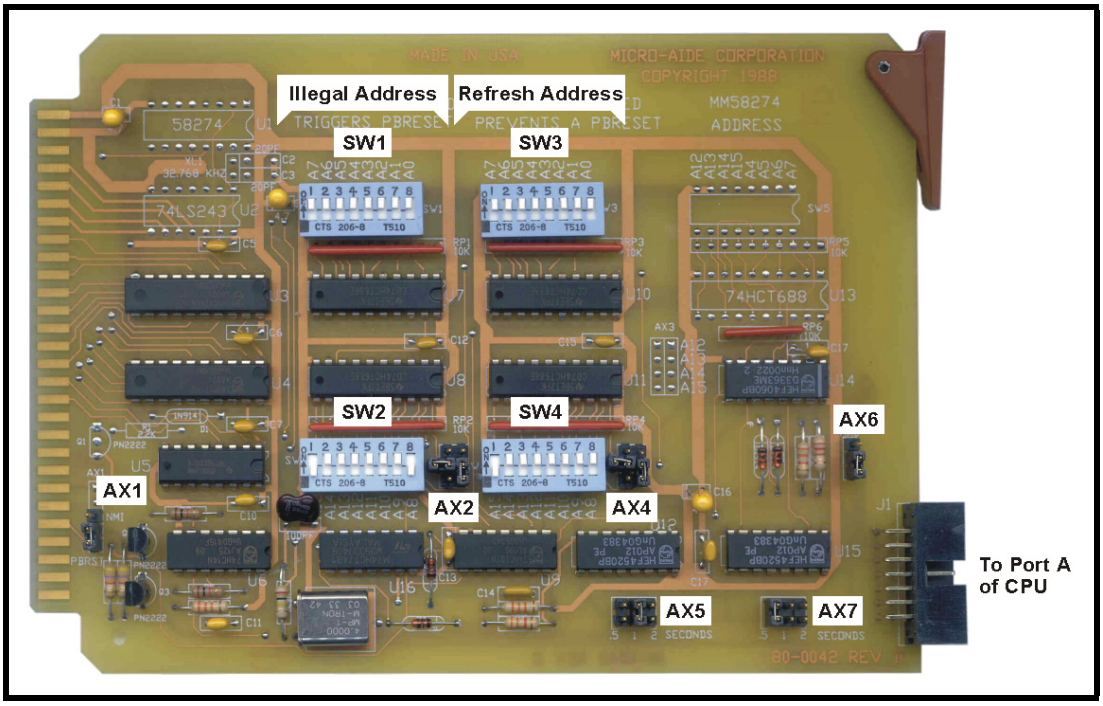


Figure 5 - 80-0042 Watchdog Timer

Operating Instructions

The Watchdog Timer does not include a programmable device of any type. However, its alarm indication can be controlled by CPU program execution or by a remote user. As described above, any access to address location 8100H will generate a system reset. Similarly, any delay longer than 1.0 seconds in accessing address location 8000H will generate a system reset. Finally, a remote user can initiate a system reset by sending a break signal longer than .5 seconds to the LCU's communications port.

80-0023 Opto-Input

Features

The 80-0023 Opto-Input is used to detect the state of inputs connected to the LCU. The LCU is equipped with five Opto-Input PCBs. Each PCB can monitor the state of 24 inputs. It can be configured for either I/O (standard) or memory mapped operation. The state of each input is read by the CPU in three groups of eight bits. Each group is assigned a consecutive address. Each Opto-Input PCB can be assigned a distinct base address.

A 4N33 opto-coupler is used to provide complete isolation of the input + and - leads. The inputs are polarity sensitive since the 4N33 only senses current in the forward direction. A 22KOhm resistor limits the current into the opto-coupler. A diode protects the opto-coupler from damage caused by excessive reverse voltage. The opto-coupler circuit is rated for operation from 10 to 50Vdc. An input voltage in this range will be validated as a logic 0 condition at the opto-coupler's output. A voltage in the range from 0 to 3Vdc will be validated as a logic 1 condition.

The + and - input leads terminate in a 50-position header connector. A ribbon cable is used to connect the input leads to a front panel connector.

Factory Configuration

The LCU is shipped with each Opto-Input PCB assigned to operate in I/O address mode. Furthermore, each PCB is assigned a unique I/O address.

Caution Do not alter the factory assigned I/O address settings for any Opto-Input PCB. If a PCB is removed from the chassis make sure it is returned to the same card slot. Failure to adhere to this procedure will cause the LCU to operate improperly.

Table 9 lists the factory settings for each PCB along with the I/O addresses associated with each group of eight inputs. Inputs 1 through 8 are read as bits 0 through 7 on the data bus. The same sequence applies to Inputs 9 through 16 and 17 through 24.

PCB No.	Card Slot No.	Address Bus						I/O Addresses		
		7	6	5	4	3	2	Inputs 1-8	Inputs 9-16	Inputs 17-24
1	4	0	0	0	0	0	0	00H	01H	02H
2	5	0	0	0	0	0	1	04H	05H	06H
3	6	0	0	0	0	1	0	08H	09H	0AH
4	7	0	0	0	0	1	1	0CH	0DH	0EH
5	8	0	0	0	1	0	0	10H	11H	12H
Switch closed (jumper on): 0 Switch open (jumper off): 1										

Table 9 - Opto-Input I/O Addresses - Factory Settings

Note Opto-Input PCBs may be assembled with an 8-position DIP switch or a jumper field in the PCB area identified as SW1.

Figure 6 on page 15 depicts the standard settings for an Opto-Input PCB assigned as PCB No. 5 (i.e., LCU inputs 97 through 120). Jumpers have been used in place of a DIP switch as described above.

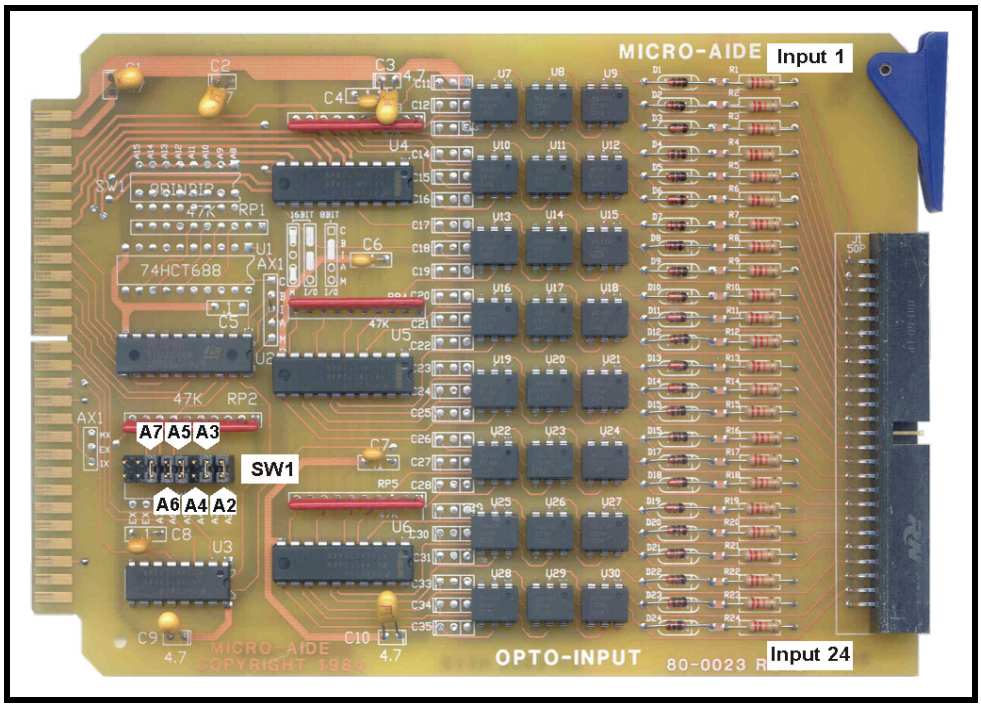


Figure 6 - 80-0023 Opto-Input

Operating Instructions

The Opto-Input does not include a programmable device of any type. Each PCB is properly configured as installed in the LCU. No adjustments to the configuration are required.

Caution In the event of a failure of an Opto-Input PCB it may become necessary to replace it with a spare PCB. In such cases the spare PCB must be configured to match the I/O addresses assigned to the failed PCB.

80-0030 Opto-Output

Features

The 80-0030 Opto-Output is used to control the state of outputs connected to the LCU. The LCU is equipped with three Opto-Output PCBs. Each PCB can control the state of 24 outputs. It can be configured for either I/O (standard) or memory mapped operation. The outputs are arranged in three groups of eight bits. Each group is assigned a consecutive address. Each Opto-Output PCB can be assigned a distinct base address. A single I/O write operation to the appropriate address will control the state of eight outputs. The bits written by the CPU are latched. Accordingly, a write operation is required only when the state of an output must be changed. A logic 0 opens the output (no current will flow). A logic 1 closes the output (current will flow).

A 4N33 opto-coupler is used to provide complete isolation of the output signals. The collector of each opto-coupler is connected to the odd numbered pins of a 50-position header connector. A ribbon cable is used to connect the output leads to a front panel connector. The emitters of all 24 opto-couplers are connected to the even numbered pins of the 50-position header connector. The common emitters are in turn connected to one contact of an on-board relay.

The second relay contact is connected to pin 50 of the 50-pin header connector. A jumper is used to enable or disable the relay-to-common-emitter connection. The relay is under control of the CPU. This feature allows the CPU to provide additional global control of all output states. The second relay contact of each Opto-Output PCB is wired within the LCU front panel to the Online Enable switch. In summary, to activate an output all of the following conditions must be satisfied.

- A logic 1 must be written to the appropriate bit and I/O address.
- The relay enable jumper must be set.
- A logic 1 must be written to the relay control latch to close the relay contacts.
- The Online Enable switch must be closed (i.e., in the up position).

The outputs are specified to operate with a 24 Vdc source. The common emitter connection through the jumper, relay contacts and Online Enable switch is connected to the return line of the 24 Vdc source.

Warning The Opto-Output does not use a series resistor to limit the flow of current through the output circuit. **The outputs must not be connected to a circuit that will result in current flow exceeding .1Adc**. A series diode is not used to protect the opto-coupler from reverse voltages. **Care should be taken not to apply reverse or negative voltages to the 24 Vdc terminals of the LCU**. Failure to do so may result in damage to the PCB.

Factory Configuration

The LCU is shipped with each Opto-Output PCB assigned to operate in I/O address mode. Furthermore, each PCB is assigned a unique I/O address.

Caution Do not alter the factory assigned I/O address settings for any Opto-Output PCB. If a PCB is removed from the chassis make sure it is returned to the same card slot. Failure to adhere to this procedure will cause the LCU to operate improperly.

Table 10 lists the factory settings for each PCB along with the I/O addresses associated with each group of eight outputs. Outputs 1 through 8 are controlled by bits 0 through 7 on the data bus. The same sequence applies to Outputs 9 through 16 and 17 through 24.

PCB No.	Card Slot No.	Address Bus						I/O Addresses			
		7	6	5	4	3	2	Outputs 1-8	Outputs 9-16	Outputs 17-24	Relay
1	9	0	1	0	0	0	0	40H	41H	42H	42H
2	10	0	1	0	0	0	1	44H	45H	46H	47H
3	11	0	1	0	0	1	0	48H	49H	4AH	48H
Switch closed (jumper on): 0 Switch open (jumper off): 1											

Table 10 - Opto-Output I/O Addresses - Factory Settings

Note Opto-Output PCBs may be assembled with an 8-position DIP switch or a jumper field in the PCB area identified as SW2.

Figure 7 on page 17 depicts the standard settings for an Opto-Output PCB assigned as PCB No. 3 (i.e., LCU outputs 49 through 72). Jumpers have been used in place of a DIP switch as described above.

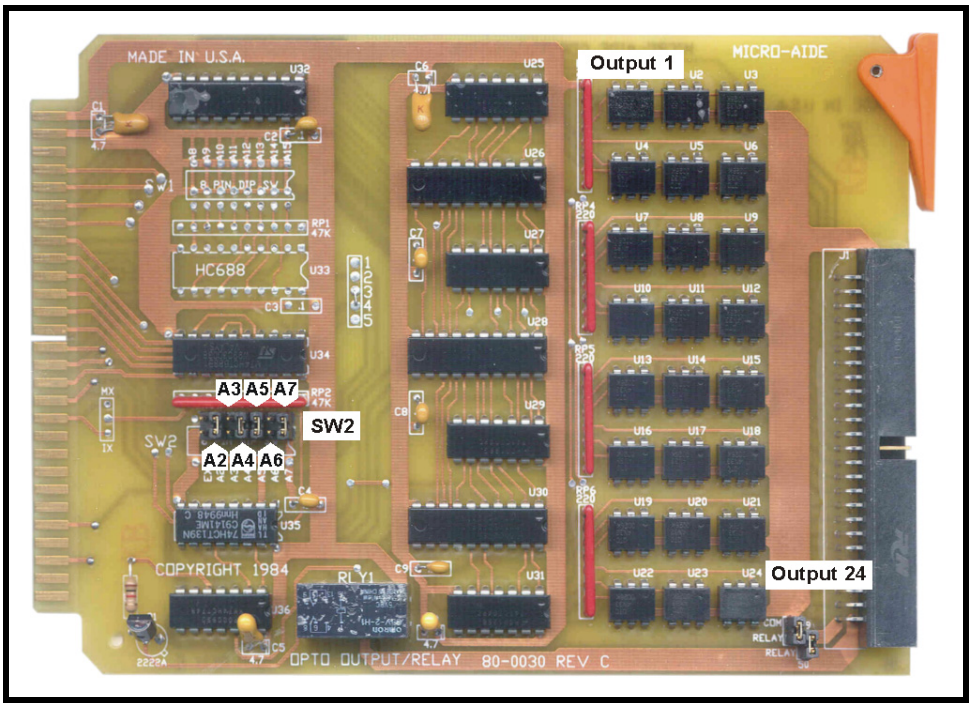


Figure 7 - 80-0030 Opto-Output

Operating Instructions

The Opto-Output does not include a programmable device of any type. Each PCB is properly configured as installed in the LCU. No adjustments to the configuration are required.

Caution In the event of a failure of an Opto-Output PCB it may become necessary to replace it with a spare PCB. In such cases the spare PCB must be configured to match the I/O addresses assigned to the failed PCB.

80-0041 Power Supply

Features

The 80-0041 Power Supply provides all of the internal power required by the LCU. It includes output voltages of 5 Vdc, 12 Vdc and -12 Vdc. It does not provide a source of the 24 Vdc required by the Opto-Input and Opto-Output PCBs. Nominal 120 Vac commercial power is applied to the Power Supply through an LCU front-panel-mounted switch. The Power Supply will operate in the range from 95 to 135 Vac at 57 to 63 Hz. An on-board step-down transformer with multiple secondary windings is used to reduce the commercial power voltage ahead of the regulator components. A series-pass regulator design was selected for the Power Supply to minimize the amount of radiated electromagnetic interference (EMI). Substantial aluminum heat sinks are used to insure adequate cooling of the regulator components. The Power Supply is designed for operation in the temperature range extending from -34°C to 74°C (-29°F to 165°F).

Note The Power Supply requires two card slots for mounting. It must be installed in card slot 13 with slot 12 left empty.

Factory Configuration

As stated above, the Power Supply includes three output voltages. The load, line regulation, load regulation and output ripple ratings for each output are listed in Table 11.

Output	Rated Load	Line Regulation	Load Regulation	Output Ripple (mVp-p)
5Vdc	3A	.5% with 10% line change	.5% with 50% load change	10
12Vdc	.5A	1% with 10% line change	1% with 50% load change	50
-12Vdc	.5A	1% with 10% line change	1% with 50% load change	50

Table 11 - Power Supply Ratings

All three outputs are protected against overload conditions. An LCU front-panel-mounted 2A fuse provides further protection of the Power Supply.

Operating Instructions

The Power Supply does not include a programmable device of any type. Each PCB is properly configured as installed in the LCU. No adjustments to the configuration are required.

80-MB13 Mother Board

The 80-MB13 Mother Board is compliant with all STD Bus requirements. As many as 13 STD Bus PCBs can be plugged into the Mother Board. However, the design of the LCU requires that only 11 of the 13 card slots be used. PCBs are inserted into the Mother Board as depicted in Figure 8.

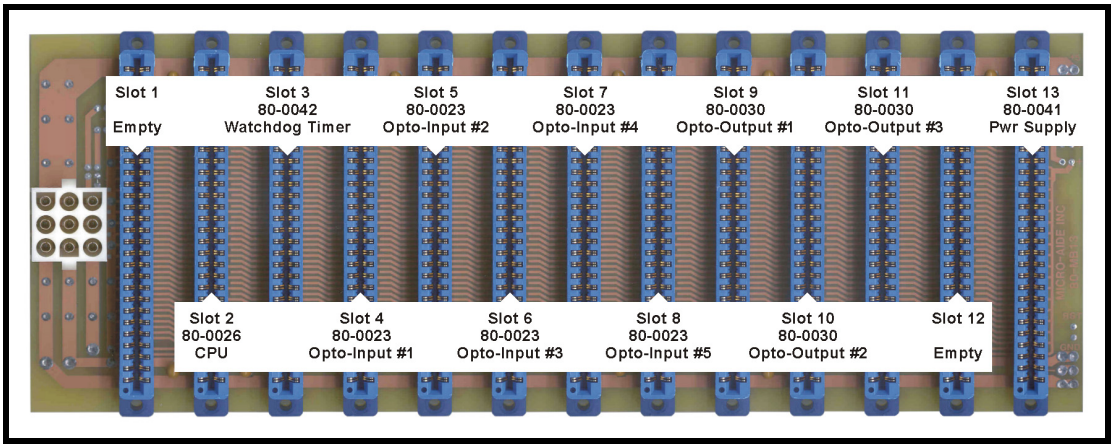


Figure 8 - 80-MB13 Mother Board

85-0010 Front Panel Interconnect

The Front Panel Interconnect assembly is secured to the inside surface of the LCU's front panel. Inputs and outputs are connected to the Opto-Input and Opto-Output PCBs via the Front Panel Interconnect assembly. A combination of circuit board traces and wire harnesses provide the following connections.

• An array of four AMP 206438-1 connectors provide termination points for all inputs and outputs. Each connector includes 57 pins.

• An array of eight 50-pin header connectors are used to interconnect the inputs and outputs via ribbon cables to the five Opto-Input and three Opto-Output PCBs.

• A 10-position header connector interconnects the Online Enable Switch Interface board and push wheel switch outputs to port C of the CPU PCB. A ribbon cable is used to bridge the connectors.

• Several screw-down terminal connectors interconnect 24Vdc power to various input and output points. They are also used to interconnect the Opto-Output PCB relays and front panel LEDs to appropriate circuit points.

Caution A set of nine ribbon cables are attached to various connectors secured to the Front Panel Interconnect assembly. If these cables are removed they must be re-installed to the same connector. Failure to do so will prevent the LCU from operating properly.

Figure 9 depicts a partially wired Front Panel Interconnect assembly.

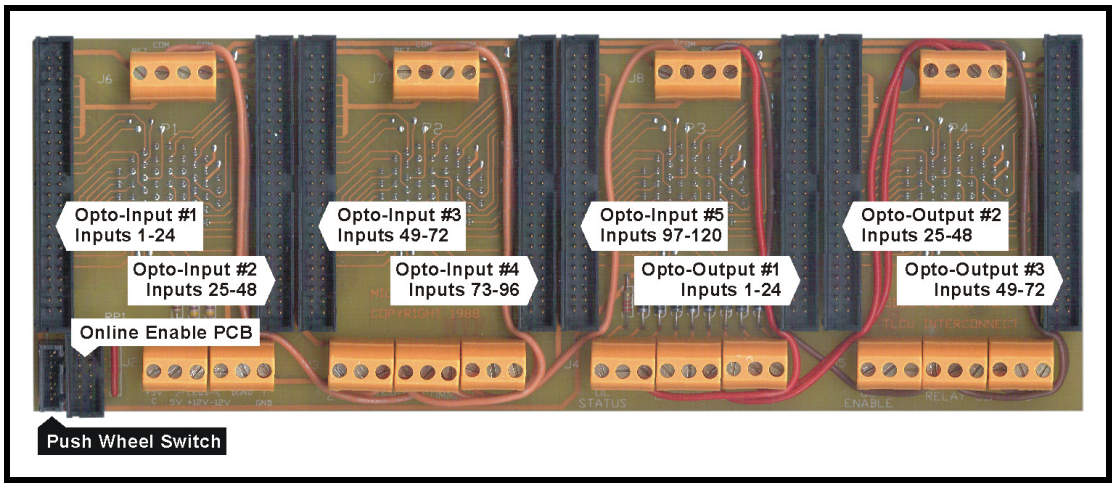


Figure 9 - 85-0010 Front Panel Interconnect

85-0086 Switch Interface

LCUs manufactured by MICRO-AIDE after July 1, 2001 include the Switch Interface. It is secured to the rear of the Online Enable switch. The Switch Interface allows the Online Enable switch to control 24Vdc power to the Opto-Output PCBs. Additionally, the on/off state of the Online Enable switch can be read as a bit via port C of the CPU. Bits 0 through 3 are used to read the hexadecimal value of the push wheel switch. Bit 4 is assigned to the Online Enable switch.

The Switch Interface includes two 10-pin header connectors. The first connector attaches to port C of the CPU. The second connector attaches to the Front Panel Interconnect assembly. Additional wires include 5Vdc and ground.

Figure 10 on page 20 depicts the Switch Interface PCB.

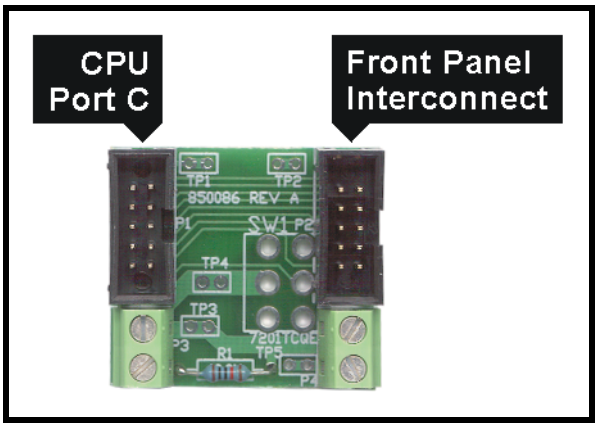


Figure 10 - 85-0086 Switch Interface

Note LCUs with serial numbers 7639 and greater include the modification that adds the Switch Interface.

CHAPTER 3

SCHEMATICS

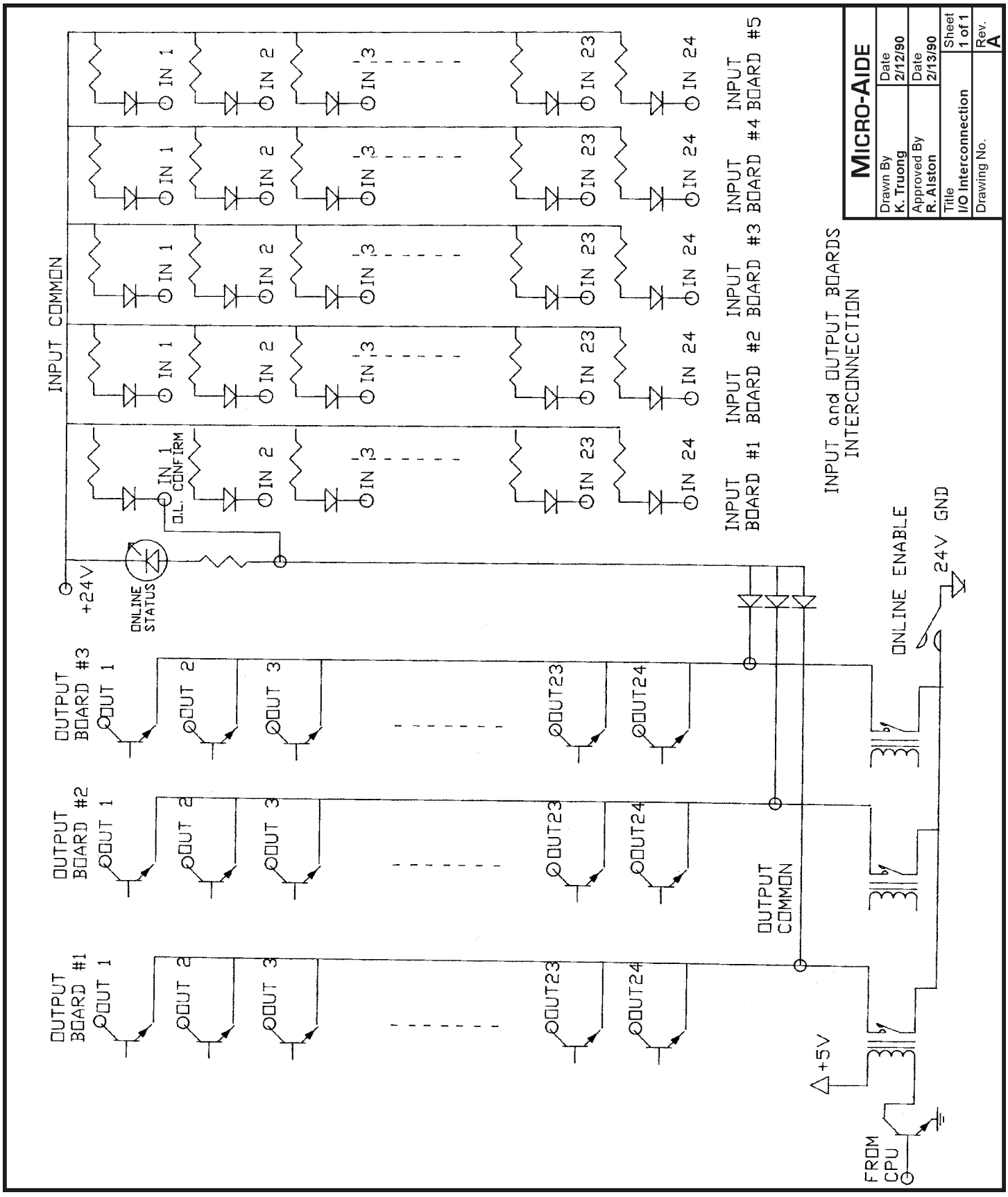
Property Rights

This chapter includes detailed schematics for each of the printed circuit boards (PCBs) used by the LCU. Except for the 85-0086 Switch Interface, all of the PCBs were designed by MICRO-AIDE. Accordingly, MICRO-AIDE retains, without qualifications, the exclusive right to manufacture these PCBs. The inclusion of these schematics within this User Manual shall not be understood as permission by MICRO-AIDE to copy any portion of the designs based upon these PCB schematics.

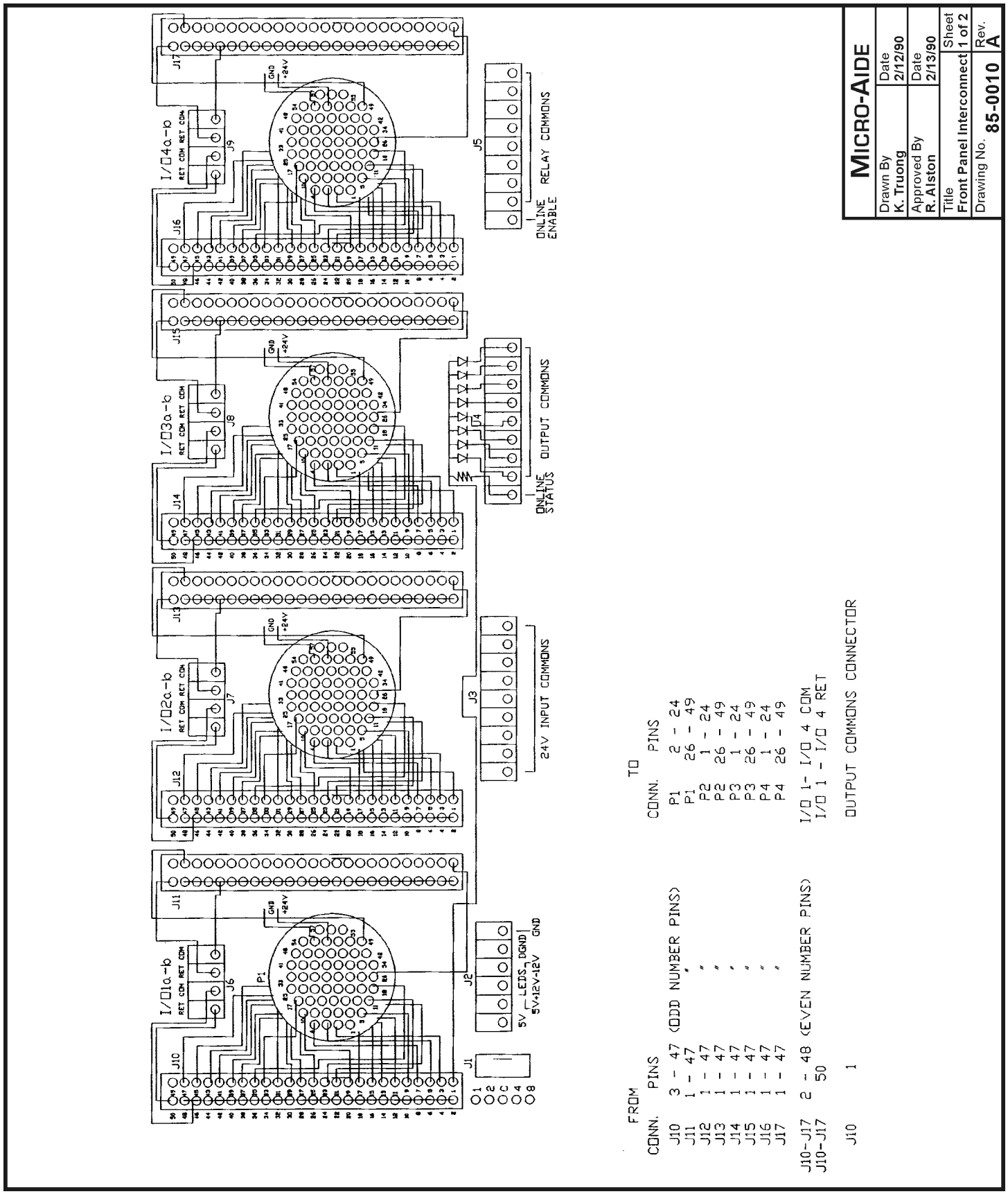
Furthermore, these schematics (except 85-0086) shall be considered the sole intellectual property of MICRO-AIDE. Their inclusion herein shall be considered as a convenience to the reader for the purposes of developing third-party firmware that will be resident in and executed by the LCU.

These schematics shall not be copied in whole or in part except as granted in writing by MICRO-AIDE.

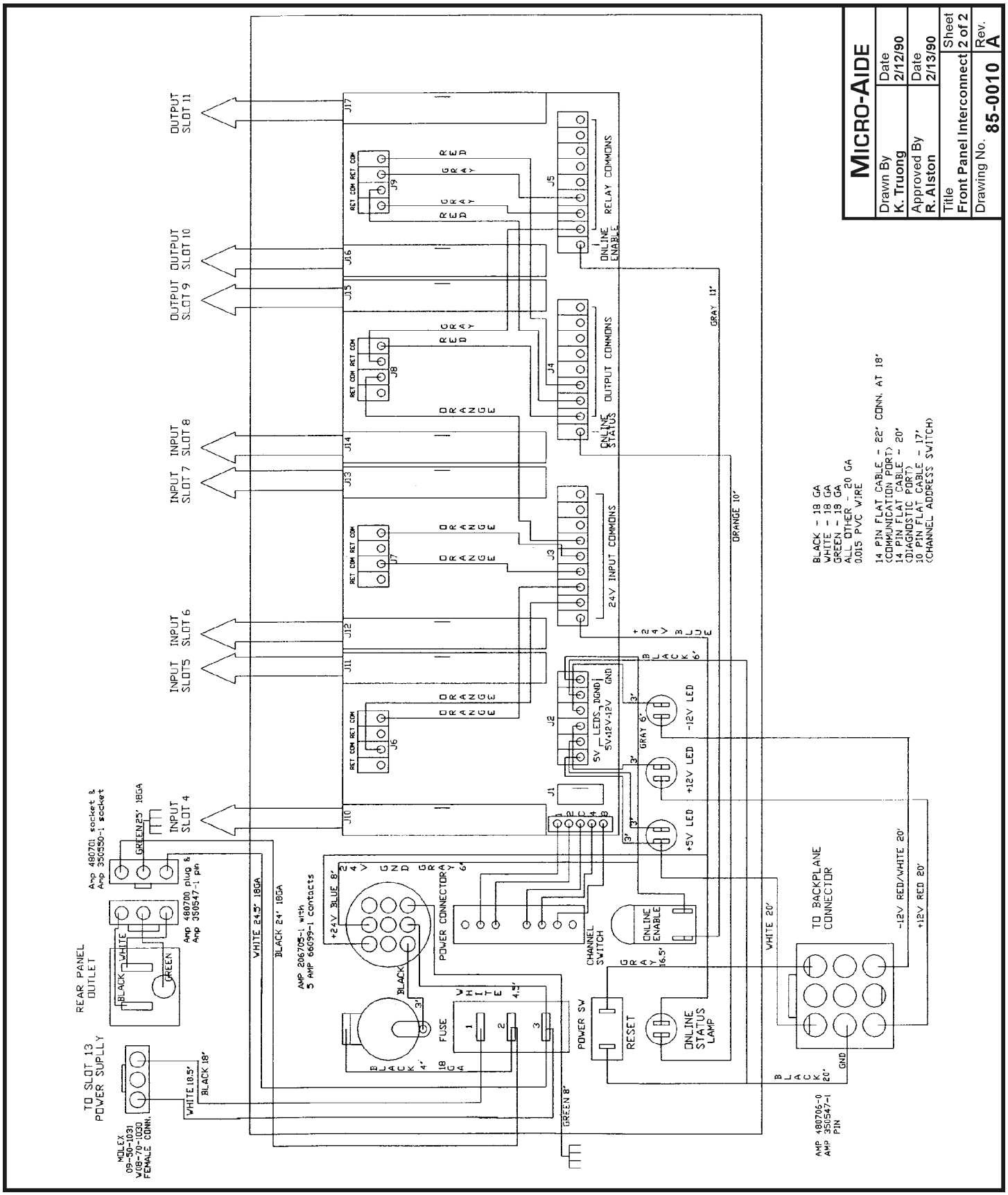
List of Drawings



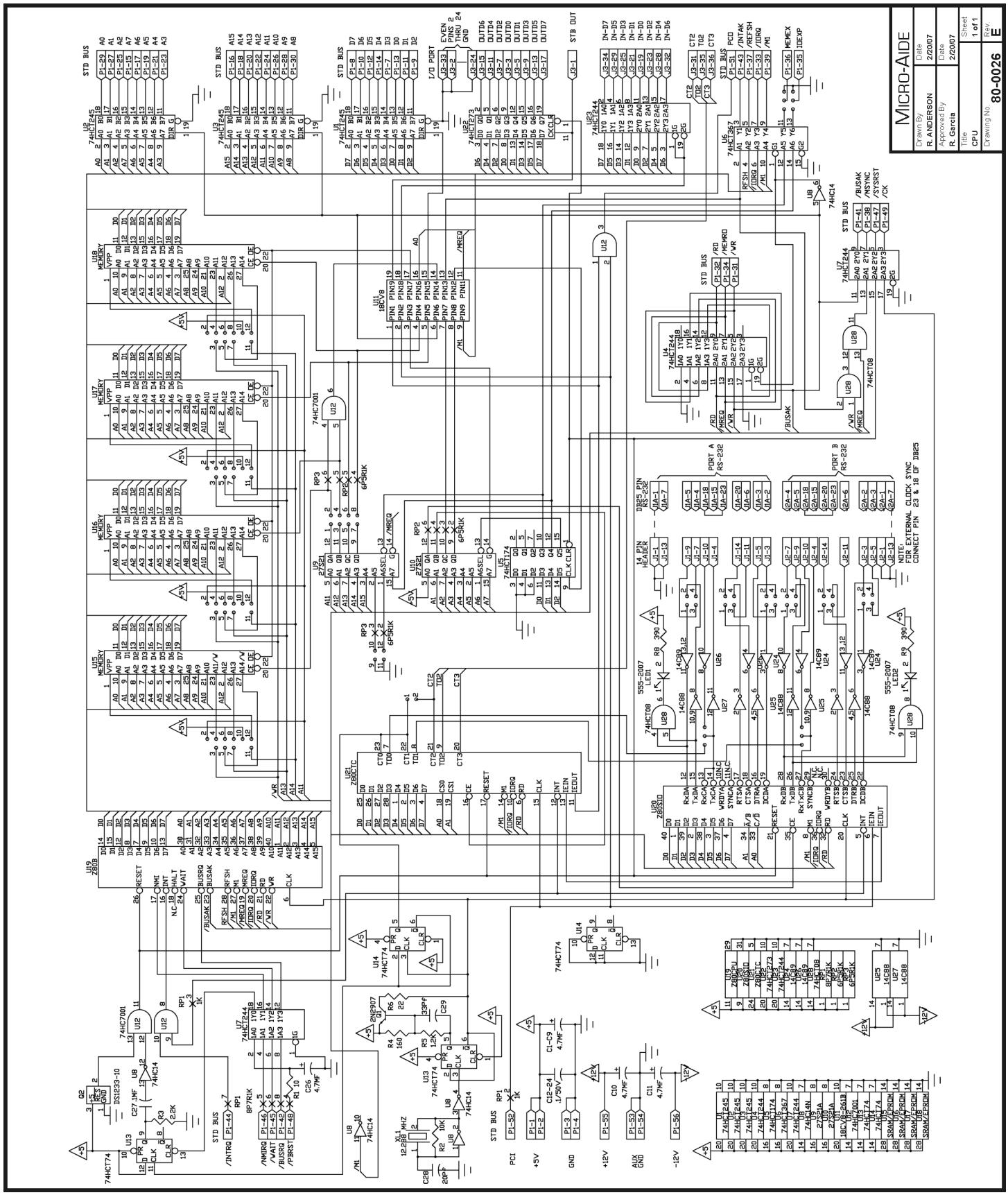
Schematic 1 - I/O Interconnection



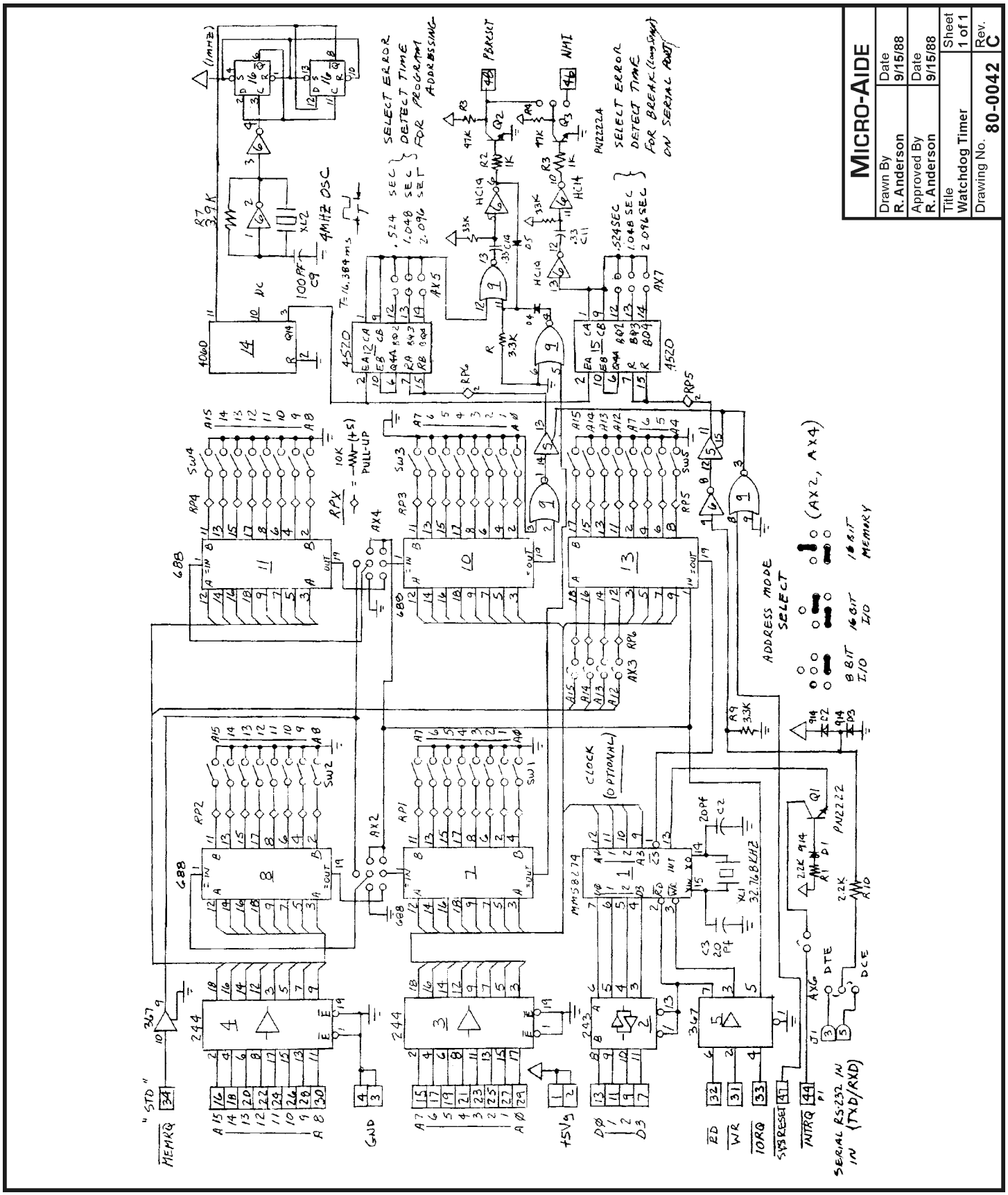
Schematic 2 - 85-0010 Front Panel Interconnect (1 of 2)



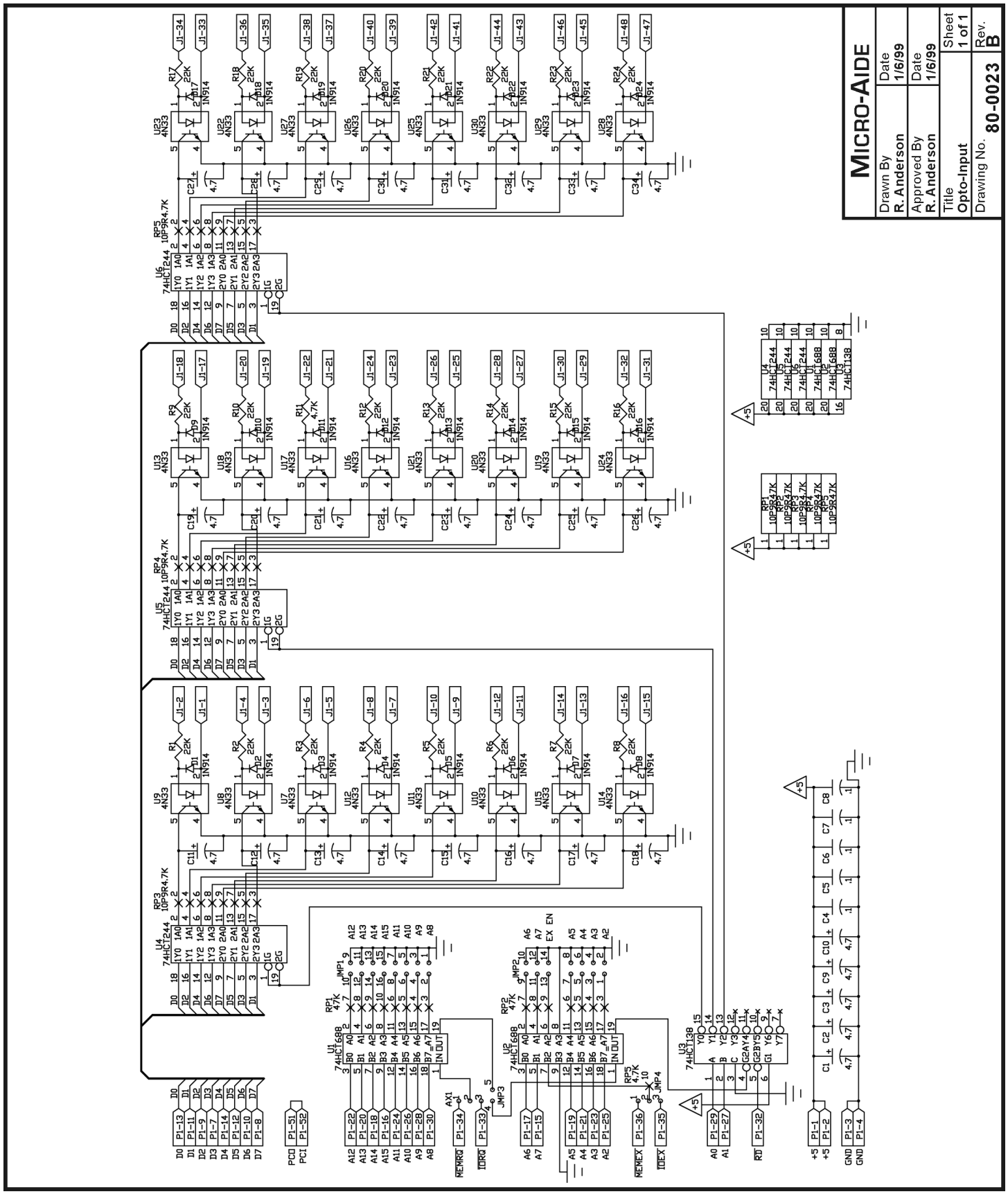
Schematic 3 - 85-0010 Front Panel Interconnect (2 of 2)



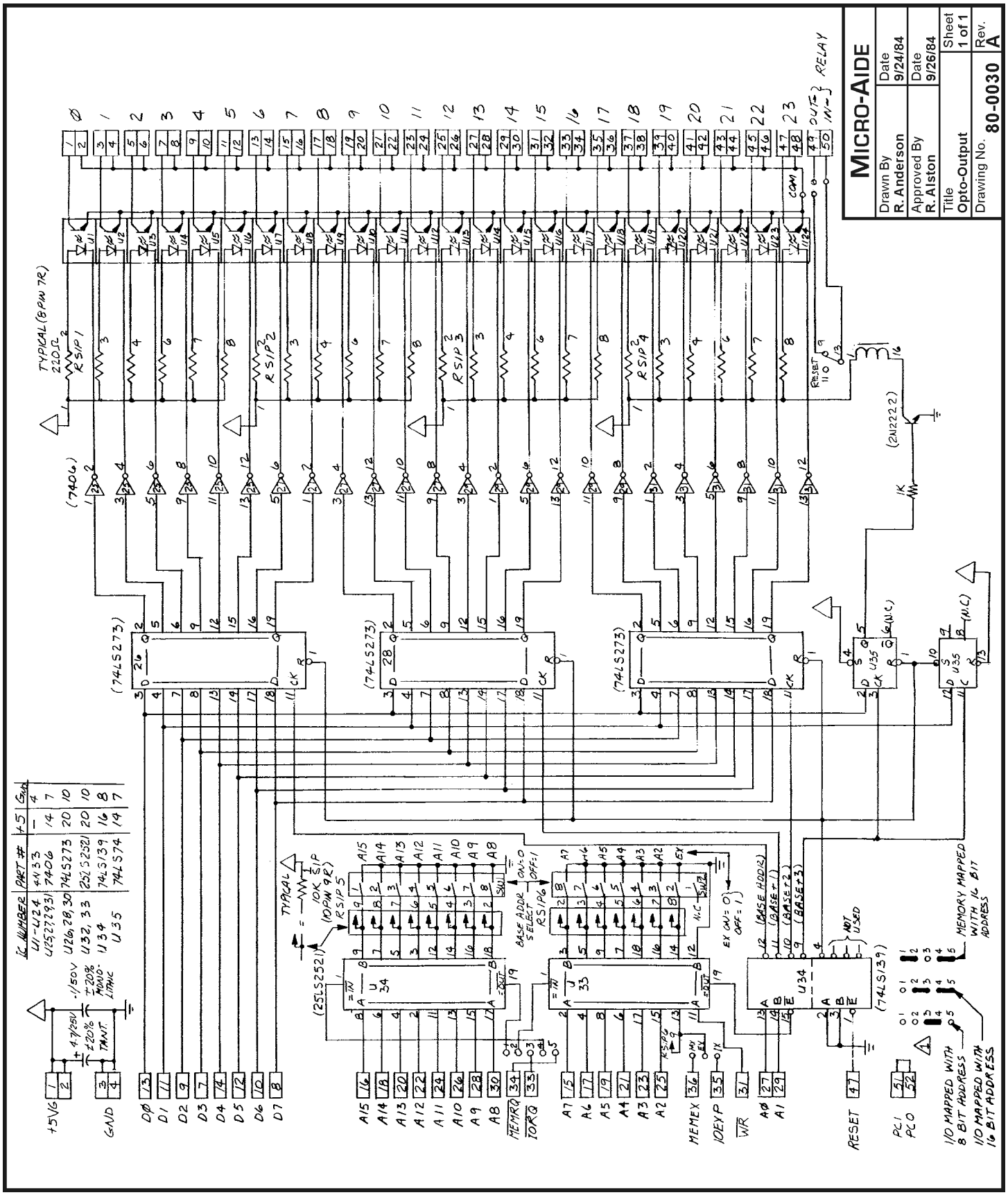
Schematic 4 - 80-0026 CPU



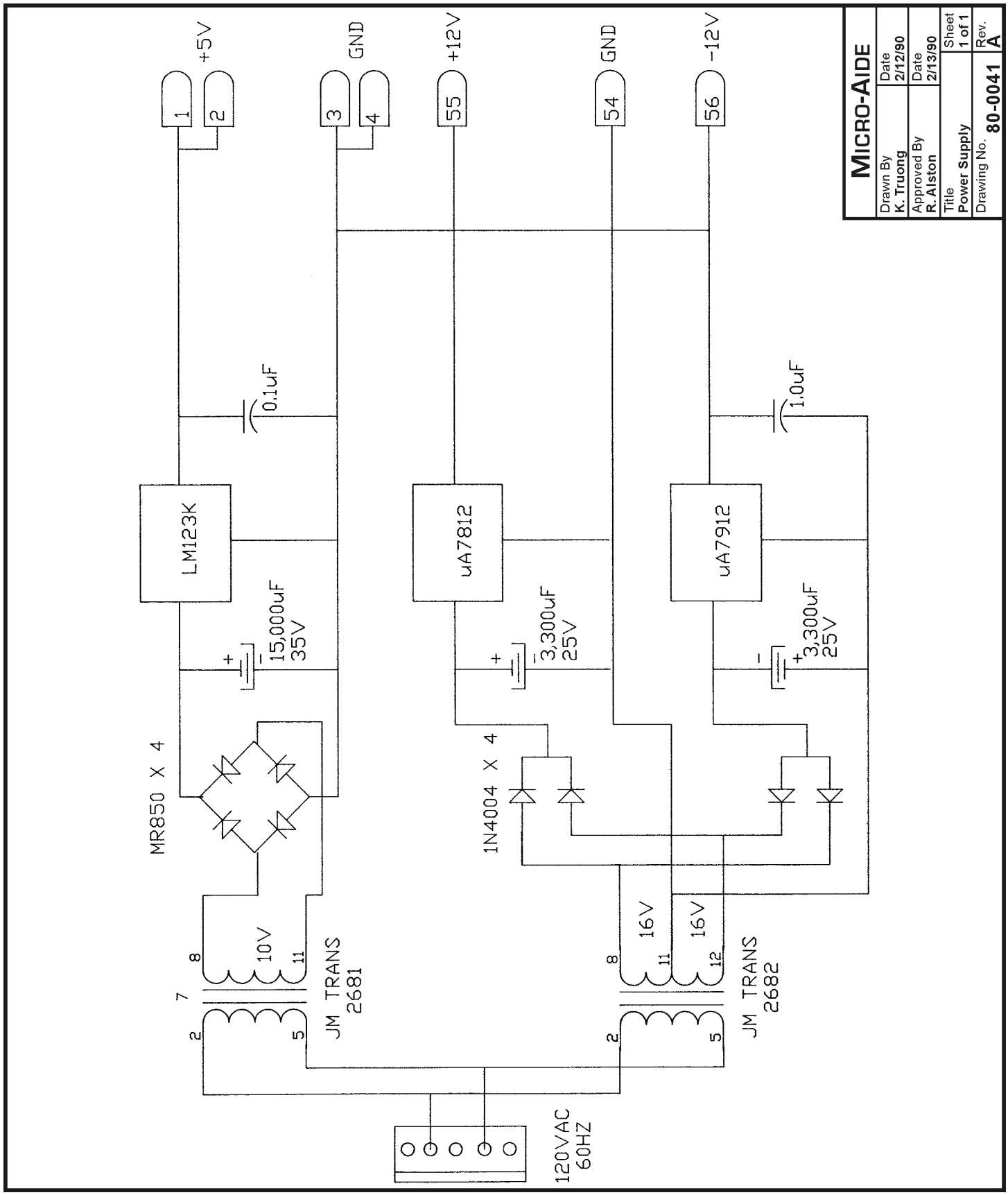
Schematic 5 - 80-0042 Watchdog Timer



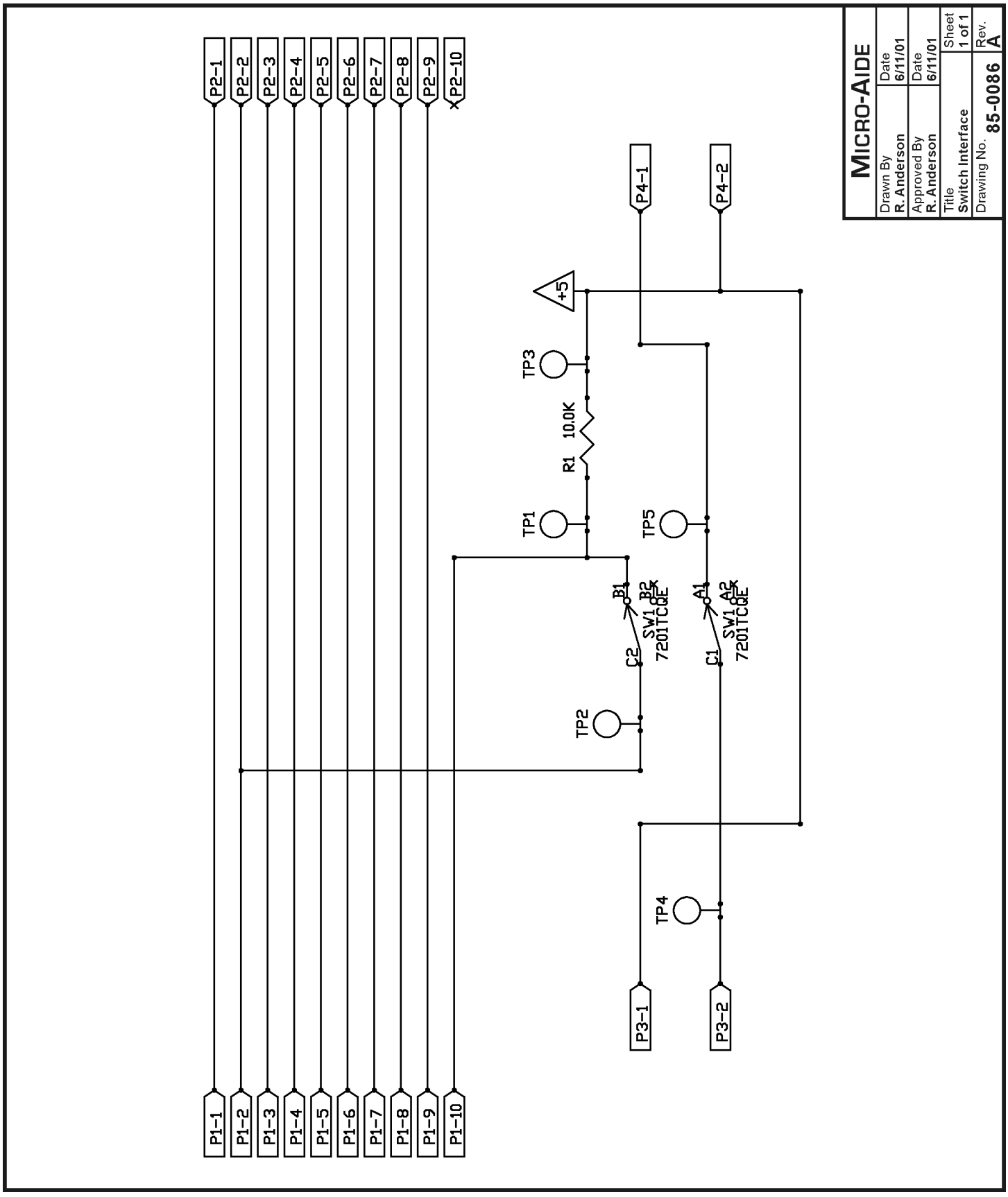
Schematic 6 - 80-0023 Opto-Input



Schematic 7 - 80-0030 Opto-Output



Schematic 8 - 80-0041 Power Supply



Schematic 9 - 85-0086 Switch Interface

TECHNICAL DATA

Specifications

Physical

Size

Length: 12.0"

Height: 5.5"

Depth: 11.9"

Weight

14lb.

Environmental

Storage

Temperature: -50°C to 85°C

Humidity: 0 to 95%, non-condensing

Operating

Temperature: -34°C to 74°C

Humidity: 0 to 95%, non-condensing

Mounting

Suitable for shelf mounting

Construction

Chassis

Fully enclosed, anodized aluminum

Externally accessible switches, LEDs and connectors

Electrical

Most components mounted on conformal coated, internal PCBs

Power

Voltages

AC: 95 to 135Vac

DC: 20 to 28Vdc

Consumption

AC: typ. 15W

DC: as required by output load, external of LCU

Fuse

AC power only, 2.5A

Capacities

Inputs

120, all opto-isolated, with common return

Outputs

72, all opto-isolated, with common return

RS-232 Port

Quantity: two, communications and diagnostic

Type: RS-232, configurable as DTE or DCE

Baud Rates: 110, 300, 1200, 2400, 4800, 9600, 19,200

Bit Format: N-8-1

Inputs

Input Impedance: 22KOhms, opto-isolated

Range - On: 10 to 50Vdc

Range - Off: 0 to 2Vdc

Outputs

Output Impedance: near zero, no series limiting resistor is used, opto-isolated

Range - On: 1Vdc drop, limit 25mAdc

Range - Off: less than .1mAdc at 24Vdc

Controls

Power: illuminated rocker, applies 120Vac

System Reset: pushbutton, restarts CPU program execution

Online Enable: toggle, enables manual control of all outputs

Channel Address: push wheel, assigns unit address in range from 1 to 16

Various switches and jumper settings on removable PCBs allow for configuration control

Indicators

Power: red, part of power switch

Online Status: red LED

Internal Power: red LEDs, one each for 5, 12 and -12Vdc

Connectors

Power

Type: single, 9-pin male, round, twist on/off, AMP 206705-1

Conductors: 5 total, AC with ground, 24Vdc and return

Input and Outputs

Type: four, 57-pin male, round, twist on/off, AMP 206438-1

Conductors: 57 per connector, to/from Opto-Input and Opto-Output PCBs

Communications Port

DB-25 female, configurable as DTE or DCE

Diagnostic Port

DB-25 female, configurable as DTE or DCE

AC Out

AC receptacle, limit 2Aac

Memory

EPROM

Single 28-pin JEDEC socket, 2 to 32KB (typ. 8KB) on CPU PCB

EEPROM

Two 28-pin JEDEC sockets, 2 to 32KB (typ. 8KB) on CPU PCB

Static RAM

Single 28-pin JEDEC socket, 2 to 32KB (typ. 32KB - 8KB used) on CPU PCB

MICRO-AIDE reserves the right to make changes, at its sole discretion, to any specifications listed herein.

User Notes

BILLS OF MATERIAL

Local Control Unit

M-A Part No.	Description / MFG Part No.	Qty.
PA80-0026/00	PCB ASSEMBLY, CPU	1
PA80-0042/00	PCB ASSEMBLY, WATCHDOG TIMER	1
PA80-0023/00	PCB ASSEMBLY, OPTO-INPUT	5
PA80-0030/00	PCB ASSEMBLY, OPTO-OUTPUT	3
PA80-0041/00	PCB ASSEMBLY, POWER SUPPLY	1
PA85-0010/00	PCB ASSEMBLY, FRONT PANEL INTERCONNECT	1
PA85-0086/00	PCB ASSEMBLY, SWITCH INTERFACE	1
PA80-MB13/00	PCB ASSEMBLY, MOTHER BOARD	1
DLSLD870/00	LED, RED, PANEL MOUNT DATA DISPLAY: PMRL200RLP2	4
F 31202.5/00	FUSE, 2.5AMP LITTELFUSE: 31202.5	1
FH34285A/00	FUSE HOLDER, PANEL MOUNT LITTELFUSE: 342858A	1
H PD-15-2/00	OUTLET, AC POWER, PANEL MOUNT POWER DYNAMICS: PD-15-2	1
HB2135/00	BUMPER, LARGE ACCURATE ELASTOMER: 2988W-034-BLK	4
HP22004/00	SUPPORT, MOTHER BOARD	2
JA102128/00	CONNECTOR PIN, FEMALE, CRIMP (TO PUSH WHEEL SWITCH) AMP: 102128-2	5
JA102241/00	CONNECTOR, FEMALE, 5-PIN (TO PUSH WHEEL SWITCH) AMP: 102241-3	1
JA205817/00	LOCKING KIT, CONNECTOR, 4-40 AMP: 205817-1	2
JA206705/00	CONNECTOR, MALE, 9-PIN, PANEL MOUNT (120VAC 24VDC) AMP: 206705-1	1
JA34107/00	TERMINAL LUG, #6 AMP: 34107	2
JA350547/00	CONNECTOR PIN, MALE (TO P/S) AMP: 350547-1	3
JA350550/00	CONNECTOR PIN, FEMALE (TO P/S) AMP: 350550-1	3
JA350690/00	CONNECTOR PIN, MALE (TO MOTHER BOARD) AMP: 350690-1	5
JA480700/00	CONNECTOR, MALE, 3-PIN (TO P/S) AMP: 1-480700-0	1
JA480701/00	CONNECTOR, FEMALE, 3-PIN (TO P/S) AMP: 1-480701-0	1

M-A Part No.	Description / MFG Part No.	Qty.
JA480706/00	CONNECTOR, MALE, 9-PIN (TO MOTHER BOARD) AMP: 1-480706-0	1
JA61687-2/00	TAB, RIGHT ANGLE, FEMALE LUG AMP: 61687-2	3
JA640905/00	TAB, STRAIGHT, FEMALE LUG AMP: 640905-1	3
JA66099/00	CONNECTOR PIN, MALE (120VAC 24VDC) AMP: 66099-1	5
JRIDDC25S/00	CONNECTOR, FEMALE, DB25, RIBBON AMP: 747303-2	2
JRIDS-C10/00	CONNECTOR, FEMALE, HEADER, 10-PIN AMP: 746285-1	6
JRIDS-C14/00	CONNECTOR, FEMALE, HEADER, 14-PIN AMP: 746285-2	3
JRIDS-C50/00	CONNECTOR, FEMALE, HEADER, 50-PIN AMP: 1-746285-0	16
JRSR-10K/00	STRAIN RELIEF, RIBBON, 10-CONDUCTOR AMP: 499252-5	6
JRSR-14K/00	STRAIN RELIEF, RIBBON, 14-CONDUCTOR AMP: 499252-9	3
JRSR-50K/00	STRAIN RELIEF, RIBBON, 50-CONDUCTOR AMP: 499252-4	16
JX8701030/00	CONNECTOR PIN, FEMALE, CRIMP MOLEX: 08-70-1030	2
JX9501031/00	CONNECTOR, FEMALE, 3-PIN MOLEX: 09-50-1031	1
M 220036/00	SHEETMETAL, SIDE PANEL	2
M 22037/00	SHEETMETAL, BOTTOM PANEL	1
M 220039/00	SHEETMETAL, FRONT PANEL	1
M 220040/00	SHEETMETAL, REAR PANEL	1
M 220057/00	SHEETMETAL, RIGHT MOUNTING BRACKET	1
M 220058/00	SHEETMETAL, TOP PANEL	1
M 220117/02	SHEETMETAL, LEFT MOUNTING BRACKET	1
M 220147/00	SHEETMETAL, NUT RING, 9-PIN CONNECTOR	1
M 220147/01	SHEETMETAL, NUT RING, 57-PIN CONNECTOR	4
SHDPS9-10/00	MOUNTING PLATE, PUSH WHEEL SWITCH ALCO: DPS9-10-P	1
SPDPS9-SG/00	SWITCH, PUSH WHEEL, 16-POSITION, PANEL MOUNT TYCO: DPS9-SG-902	1
SPMB2411/00	SWITCH, PUSHBUTTON, PANEL MOUNT NKK: MB2411JW01-C-1A	1
SRXRL110A/00	SWITCH, ROCKER, SPST, PANEL MOUNT AMP: 1571092-1	1
ZMTCLU-1	USER MANUAL, LCU	1

Printed Circuit Boards

PA80-0026 CPU PCB (Rev E)

M-A Part No.	Description / MFG Part No.	Qty.
P 80-0026/00	PCB, CPU	1
C .1MF/00	CAPACITOR, .1MF, 50V, CERAMIC	15
CM20PF/00	CAPACITOR, 20PF, 100V, MICA SAHA: DM10-200J	1
CM33PF/00	CAPACITOR, 33PF, 100V, MICA SAHA: DM10-330J	1
CT4.7MF/00	CAPACITOR, 4.7MF, 25V, RADIAL, TANTALUM	11
DL5350T1/00	LED, RED, RIGHT ANGLE CHICAGO MINIATURE: 5350T1	2
HECPU/00	EJECTOR, WHITE, CPU PHILLIPS COMPONENTS: E-5-9	1
JPWW18-2R/00	WIREWRAP PINS, 18 BY 2 SAMTEC: TSW11807LD	2
JPWW36-1R/00	WIREWRAP PINS, 36 BY 1 SAMTEC: TSW13607LS	2
JRICO-143/00	SOCKET, IC, 14-PIN OUPIIN: 8003-14T3U-SN	4
JRICO-163/00	SOCKET, IC, 16-PIN OUPIIN: 8003-16T3U-SN	2
JRICO-203/00	SOCKET, IC, 20-PIN OUPIIN: 8003-20T3U-SN	1
JRICO-286/00	SOCKET, IC, 28-PIN OUPIIN: 8003-28T6U-SN	5
JRICO-406/00	SOCKET, IC, 40-PIN OUPIIN: 8003-40T6U-SN	2
JRIDH10LP/00	CONNECTOR, HEADER, 10-PIN, RIGHT ANGLE OUPIIN: 3012-10GRB	1
JRIDH14LP/00	CONNECTOR, HEADER, 14-PIN, RIGHT ANGLE OUPIIN: 3012-14GRB	2
Q 2N2907/00	TRANSISTOR, PNP 2N2907	1
R 10 OHM/00	RESISTOR, 10 OHM, 5%, .25W	1
R 22 OHM/00	RESISTOR, 22 OHM, 5%, .25W	1
R 160 OHM/00	RESISTOR, 160 OHM, 5%, .25W	1
R 390 OHM/00	RESISTOR, 390 OHM, 5%, .25W	2
R 1.2K/00	RESISTOR, 1.2K, 5%, .25W	1
R 2.2K/00	RESISTOR, 2.2K, 5%, .25W	1
R 5.6K/00	RESISTOR, 5.6K, 5%, .25W	1
R 10K/00	RESISTOR, 10K, 5%, .25W	1
RN6S1K/01	RESISTOR NETWORK, 6-PIN, SIP, 1K, 2% BI TECHNOLOGIES: L061C102	2
RN8S1K/01	RESISTOR NETWORK, 8-PIN, SIP, 1K, 2% BI TECHNOLOGIES: L081C102	1
U 14C88IN/00	IC, RS-232 DRIVER, DIP TI: SN75C188AN	2

M-A Part No.	Description / MFG Part No.	Qty.
U 14C89IN/00	IC, RS-232 RECEIVER, DIP TI: SN75C189AN	2
U DS1233/00	IC, POWER RESET DALLAS SEMICONDUCTOR: DS1233-10	1
UM27C64/00	IC, EPROM, 8K BY 8, DIP SGS: M27C64A-15F1	1
UM28C64/00	IC, EEPROM, 8K BY 8, DIP ATMEL: AT28C64B15-PI	2
UM82S131/00	PROM, 512 BY 4, DIP AMD: AM27S21PC	2
UR43256/00	IC, STATIC RAM, 32K BY 8, DIP CYPRESS: CY62256L-70PC	1
UP18CV8/06	PEEL, 85C, DIP ICT: 18CV8PI-15	1
USHC14/00	IC, HEX INVERTER, DIP TI: SN74HC14N	1
USHC240/00	IC, OCTAL BUS DRIVER, INVERTER, DIP TI: SN74HC240N	1
USHC367/00	IC, HEX BUFFER DRIVER, DIP TI: SN74HC367N	1
USHC7001/00	IC, QUAD AND GATE, DIP SN74HC7001N	1
USHCT08/00	IC, QUAD AND GATE, DIP SN74HCT08N	1
USHCT174/00	IC, HEX LATCH, DIP TI: SN74HCT174N	1
USHCT244/00	IC, OCTAL BUS DRIVER, DIP TI: SN74HCT244N	2
USHCT245/00	IC, OCTAL BUS TRANSCEIVER, DIP TI: SN74HCT245N	3
USHCT74/00	IC, DUAL FLIP-FLOP, DIP TI: SN74HCT74N	2
UZ84C006/00	IC, ZILOG Z80B MICROPROCESSOR, 6MHZ, DIP ZILOG: 84C0006PEC	1
UZ84C3006/00	IC, ZILOG Z80B CTC, 6MHZ, DIP ZILOG: 84C3006PEC	1
UZ84C4006/00	IC, ZILOG Z80B SIO, 6MHZ, DIP ZILOG: 84C4006PEC	1
X 12.288/00	CRYSTAL, 12.288MHZ STD: 800R-12.288-18	1

PA80-0042 Watchdog Timer PCB

M-A Part No.	Description / MFG Part No.	Qty.
P 80-0042/00	PCB, WATCHDOG TIMER	1
C .1MF/00	CAPACITOR, .1MF, 50V, CERAMIC	10
C .33MF/00	CAPACITOR, .33MF, 50V, CERAMIC	1
CM20PF/00	CAPACITOR, 20PF, 100V, MICA SAHA: DM10-200J	1
CT4.7MF/00	CAPACITOR, 4.7MF, 25V, RADIAL, TANTALUM	3
D 1N914/00	DIODE IN914	4

M-A Part No.	Description / MFG Part No.	Qty.
HEWD-TIME/00	EJECTOR, BROWN, WD-TIME PHILLIPS COMPONENTS: E-5-1	1
JPWW18-2R/00	WIREWRAP PINS, 18 BY 2 SAMTEC: TSW11807LD	1
JPWW36-1R/00	WIREWRAP PINS, 36 BY 1 SAMTEC: TSW13607LS	1
JRIDH14LP/00	CONNECTOR, HEADER, 14-PIN, RIGHT ANGLE OUPIIN: 3012-14GRB	1
Q PN2222A/00	TRANSISTOR, TO-92 PN2222	1
RN10S10K/00	RESISTOR NETWORK, 10-PIN, SIP, 10K, 2% BI TECHNOLOGIES: L101C103	5
R 1K/00	RESISTOR, 1K, 5%, .25W	2
R 2.2K/00	RESISTOR, 2.2K, 5%, .25W	1
R 3.3K/00	RESISTOR, 3.3K, 5%, .25W	2
R 4.7K/01	RESISTOR, 4.7K, 5%, .25W	2
R 33K/00	RESISTOR, 33K, 5%, .25W	2
R 200K/00	RESISTOR, 200K, 5%, .25W	2
RN10S10K/00	RESISTOR NETWORK, 10-PIN, SIP, 10K, 2% BI TECHNOLOGIES: L101C103	5
RN6S10K/00	RESISTOR NETWORK, 6-PIN, SIP, 10K, 2% BI TECHNOLOGIES: L061C103	1
SD8SPST/00	SWITCH, 8-POSITION, DIP AMP: 3-435640-9	4
SH4352385/00	SWITCH COVER, 8-POSITION, DIP GRAYHILL: 76P08	4
U 4060/00	IC, DIVIDER, DIP MOTOROLA: MC14060BCP	1
U 4520/00	IC: COUNTER, DIP MOTOROLA: MC14520BCP	2
USHC14/00	IC, HEX INVERTER, DIP TI: SN74HC14N	1
USHC367/00	IC, HEX BUFFER DRIVER, DIP TI: SN74HC367N	1
USHCT02/00	IC, QUAD OR GATE, DIP TI: SN74HCT02	1
USHCT244/00	IC, CMOS, OCTAL BUS DRIVER, DIP TI: SN74HCT244N	2
USHCT688/00	IC, CMOS, 8-BIT COMPARATOR, DIP TI: SN74HCT688N	4
USHCT74/00	IC, DUAL FLIP-FLOP, DIP TI: SN74HCT74N	1
X 4.00/00	CRYSTAL, 4.00MHZ ABRACON: AB-4.000MHZ-B2	1

PA80-0023 Opto-Input PCB

M-A Part No.	Description / MFG Part No.	Qty.
P 80-0023/00	PCB, OPTO-INPUT	1
C .1MF/00	CAPACITOR, .1MF, 50V, CERAMIC	5
CT4.7MF/00	CAPACITOR, 4.7MF, 25V, RADIAL, TANTALUM	5

M-A Part No.	Description / MFG Part No.	Qty.
D 1N914/00	DIODE IN914	24
HEDC-IN/00	EJECTOR, BLUE, DC-IN PHILLIPS COMPONENTS: E-5-6	1
JPWW18-2R/00	WIREWRAP PINS, 18 BY 2 SAMTEC: TSW11807LD	1
JRIDH50LP/00	CONNECTOR, HEADER, 50-PIN, RIGHT ANGLE OUPIIN: 3012-50GRB	1
R 22K/00	RESISTOR, 22K, 5%, .25W	24
RN10S4.7K/00	RESISTOR NETWORK, 10-PIN, SIP, 4.7K, 2% BI TECHNOLOGIES: L101C472	3
RN10S47K/00	RESISTOR NETWORK, 10-PIN, SIP, 47K, 2% BI TECHNOLOGIES: L101C473	1
UO4N33/00	IC, OPTO-COUPLER, SINGLE, DIP FAIRCHILD: 4N33	24
USHCT138/00	IC, CMOS, OCTAL DECODER, DIP TI: SN74HCT138N	1
USHCT244/00	IC, CMOS, OCTAL BUS DRIVER, DIP TI: SN74HCT244N	3
USHCT688/00	IC, CMOS, 8-BIT COMPARATOR, DIP TI: SN74HCT688N	1

PA80-0030 Opto-Output PCB

M-A Part No.	Description / MFG Part No.	Qty.
P 80-0030/00	PCB, OPTO-OUTPUT	1
C .1MF/00	CAPACITOR, .1MF, 50V, CERAMIC	5
CT4.7MF/00	CAPACITOR, 4.7MF, 25V, RADIAL, TANTALUM	4
HEDC-OUT/00	EJECTOR, ORANGE, DC-OUT PHILLIPS COMPONENTS: E-5-3	1
JPWW18-2R/00	WIREWRAP PINS, 18 BY 2 SAMTEC: TSW11807LD	1
JPWW36-1R/00	WIREWRAP PINS, 36 BY 1 SAMTEC: TSW13607LS	1
JRIDH50LP/00	CONNECTOR, HEADER, 50-PIN, RIGHT ANGLE OUPIIN: 3012-50GRB	1
K G5V-2/00	RELAY, 5V, DIP OMRON: G5V-2-H1-DC5	1
Q PN2222A/00	TRANSISTOR, TO-92 PN2222	1
R 1K/00	RESISTOR, 1K, 5%, .25W	1
RN10S47K/00	RESISTOR NETWORK, 10-PIN, SIP, 47K, 2% BI TECHNOLOGIES: L101C473	1
RN8S220/00	RESISTOR NETWORK, 8-PIN, SIP, 220 OHM, 2% BI TECHNOLOGIES: L081C221	4
UO4N33/00	IC, OPTO-COUPLER, SINGLE, DIP FAIRCHILD: 4N33	24
USACT04/00	IC, HEX INVERTER, HIGH CURRENT, DIP TI: SN74ACT04	4
USHCT139/00	IC, CMOS, DUAL 4-BIT DECODER, DIP TI: SN74HCT139N	1

M-A Part No.	Description / MFG Part No.	Qty.
USHCT244/00	IC, CMOS, OCTAL BUS DRIVER, DIP TI: SN74HCT244N	1
USHCT273/00	IC, CMOS, OCTAL LATCH, DIP TI: SN74HCT273N	3
USHCT688/00	IC, CMOS, 8-BIT COMPARATOR, DIP TI: SN74HCT688N	1
USHCT74/00	IC, DUAL FLIP-FLOP, DIP TI: SN74HCT74N	1

PA80-0041 Power Supply PCB

M-A Part No.	Description / MFG Part No.	Qty.
P 80-0041/00	PCB, POWER SUPPLY	1
C .1MF/00	CAPACITOR, .1MF, 50V, CERAMIC	1
C 1MF/00	CAPACITOR, 1MF, 50V, CERAMIC	1
CE3300MF/00	CAPACITOR, 3300MF, 50V, RADIAL, ELECTROLYTIC NICHICON: LLK1V332MHSZ	2
CE6800MF/00	CAPACITOR, 6800MF, 25V, RADIAL, ELECTROLYTIC NICHICON: LGK1V682MHSZ	1
D 1N4004/00	DIODE, 400V 1N4004	4
D MR850/00	DIODE, POWER MOTOROLA: MR850	4
HEPOWER/00	EJECTOR, RED, POWER PHILLIPS COMPONENTS: E-5-2	1
HS5072B/00	HEAT SINK AAVID: 507222B	2
JA34107/00	TERMINAL LUG, #6 AMP: 34107	1
JX2660403/00	CONNECTOR, MALE, 3-PIN, POWER MOLEX: 26-60-4030	1
M 220056/00	SHEETMETAL, HEAT SINK	1
QR7812/00	VOLTAGE REGULATOR, 12V, NATIONAL: LM7812CT	1
QR7912/00	VOLTAGE REGULATOR, -12V, NATIONAL: LM7912CT	1
QRLM323K/00	VOLTAGE REGULATOR, 5V NATIONAL: LM323K	1
T 2681/00	TRANSFORMER, 10V 3AMP JM TRANSFORMER: 2681	1
T 2682/00	TRANSFORMER, 32V 3AMP, CENTER TAP JM TRANSFORMER: 2682	1

PA85-0010 Front Panel Interconnect PCB

M-A Part No.	Description / MFG Part No.	Qty.
P 85-0010/00	PCB, FRONT PANEL INTERCONNECT	1
D 1N4004/00	DIODE, 400V 1N4004	8
JA102202/00	CONNECTOR, HEADER, 5-PIN, STRAIGHT ANGLE AMP: 102202-2	1
JA206438/00	CONNECTOR, FEMALE, 57-PIN, ROUND AMP: 206438-1	4

M-A Part No.	Description / MFG Part No.	Qty.
JA206509/00	PLUG, KEYING AMP: 206509-1	4
JA745288/00	CONTACT PIN, SOCKET AMP: 745288-6	228
JRIDH10LP/01	CONNECTOR, HEADER, 10-PIN, STRAIGHT ANGLE OUPIIN: 3012-10GSB	1
JRIDH50LP/01	CONNECTOR, HEADER, 50-PIN, STRAIGHT ANGLE OUPIIN: 3012-50GSB	8
JW159455/00	CONNECTOR, SCREW-DOWN, FEMALE, 3-POSITION WEIDMULLER: 159455	11
JW995132/00	CONNECTOR, SCREW-DOWN, FEMALE, 4-POSITION WEIDMULLER: 995132	4
R 180 OHM/00	RESISTOR, 180 OHM, 5%, .25W	1
R 470 OHM/00	RESISTOR, 470 OHM, 5%, .25W	2
R 2.2K/00	RESISTOR, 2.2K, 5%, .25W	1
RN6S10K/00	RESISTOR NETWORK, 6-PIN, SIP, 10K, 2% BI TECHNOLOGIES: L061C103	1

PA85-0086 Switch Interface PCB

M-A Part No.	Description / MFG Part No.	Qty.
P 85-0086/00	PCB, SWITCH INTERFACE	1
J 1729128/00	CONNECTOR, FEMALE, 2-POSITION, SCREW-DOWN PHOENIX CONTACT: 1729128	2
JRIDH10LP/01	CONNECTOR, HEADER, 10-PIN, STRAIGHT ANGLE OUPIIN: 3012-10GSB	2
JRIDS-C10/00	CONNECTOR, 10-PIN, FEMALE F/W AMP: 746285-1	4
JRSR-10K/00	STRAIN RELIEF, RIBBON, 10-CONDUCTOR AMP: 499252-5	4
R 10K/00	RESISTOR, 10K, 5%, .25W	1
ST7201TCQ/00	SWITCH, TOGGLE, SPDT, PCB MOUNT C&K: 7201TCQE	1

PA80-MB13 Mother Board PCB

M-A Part No.	Description / MFG Part No.	Qty.
P 80-MB13/00	PCB, MOTHER BOARD, 13-SLOT	1
CT4.7MF/00	CAPACITOR, 4.7MF, 25V, RADIAL, TANTALUM	9
JA350763/00	CONNECTOR, 9-PIN, POWER AMP: 350763-4	1
JCEZA28/00	CONNECTOR, 56-PIN, CARD EDGE SULLINS: EZA28DCTD	13

Material Return Policy

In the event the customer identifies a malfunction in any product, call or write MICRO-AIDE and obtain a Return Material Authorization (RMA) number from the customer service department. Return the product to MICRO-AIDE, freight prepaid, with a note (in-warranty repair) or a purchase order (out-of-warranty) for the repair listing the following information:

- RMA number from MICRO-AIDE
- Return shipment address
- Name and telephone number of person familiar with the problem
- Brief description of the problem (include any printouts that may have a bearing on the problem)
- Method of payment for repair costs (out-of-warranty)
- Send product to the following address:

MICRO-AIDE CORPORATION
685 Arrow Grand Circle
Covina, CA 91722
Tel: 626-915-5502 Fax: 626-331-9484
E-mail: support@micro-aide.com

Limited Warranty

MICRO-AIDE warrants its products to be free from defects in material and workmanship for a period of five (5) years from the date of shipment. This warranty is in lieu of any other warranty, expressed or implied. In no event shall MICRO-AIDE be held liable for incidental or consequential damage resulting from (1) the use of any of its products, or (2) any alleged breach of this warranty provision. MICRO-AIDE's liability shall be limited to repairing or replacing, at its sole discretion, any defective product which is returned in accordance with the MICRO-AIDE Material Return Policy.

Product that has been subjected to abuse, misuse, alteration, accident, lightning damage, neglect or unauthorized installation or repair shall not be covered by this warranty. MICRO-AIDE reserves the right to make a final decision as to the existence of any failures and the cause of such failures. No warranty is made with respect to custom equipment or products produced to buyer's specifications except as mutually agreed upon in writing.

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